

# 2010 Design Engineer's Guide to OpenVPX

OpenVPX - From Concept to Specification

Transitioning to OpenVPX for Next-Generation C4ISR Systems

Putting OpenVPX to Work

Who's Who In OpenVPX



Supplement to *Embedded Technology*



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## Let the Show Begin

VPX is like a three act play. Act one was the launching of a new high density platform for critical embedded computing applications. Leveraging the wildly popular VMEbus in 3U and 6U Eurocard formats, VPX added the capability of using high speed serial switch fabric technologies such as Ethernet, PCI Express, serial RapidIO, and others, that can be configured in various backplane topologies. VPX also greatly increased the number of backplane pins to handle more data traffic and user I/O making it more effective for today's applications.

Act two was the addition of an architectural framework that manages and constrains module and backplane designs, including defining pin outs, and that sets interoperability points within VPX while maintaining full compliance. This architectural framework is referred to as OpenVPX™. It was recently ratified by VITA and ANSI, making it available to the general public.

The efforts of the OpenVPX (VITA 65) working group represent a significant shift in the industry. Major industry buyers came to VITA to get an architectural framework for VPX in place, and quickly. The team responded start to finish in less than 14 months, which is quite incredible given the scope of the project. Much work is still ahead as additional framework alternatives are defined to meet specific needs of new applications of the VPX technology.

Act three is the rollout of products, from boards to complete systems, that follow the family of VPX specifications. Over 30 companies have announced, or plan to announce, products based on the series of specifications that define VPX. During this act, there will be much jockeying for position as the various profiles defined in OpenVPX (ANSI/VITA65.0-2010) start to gain acceptance. Trends will emerge that point to specific serial switch fabrics, board/system sizes, interconnect topologies, and many other configuration options possible with VPX.

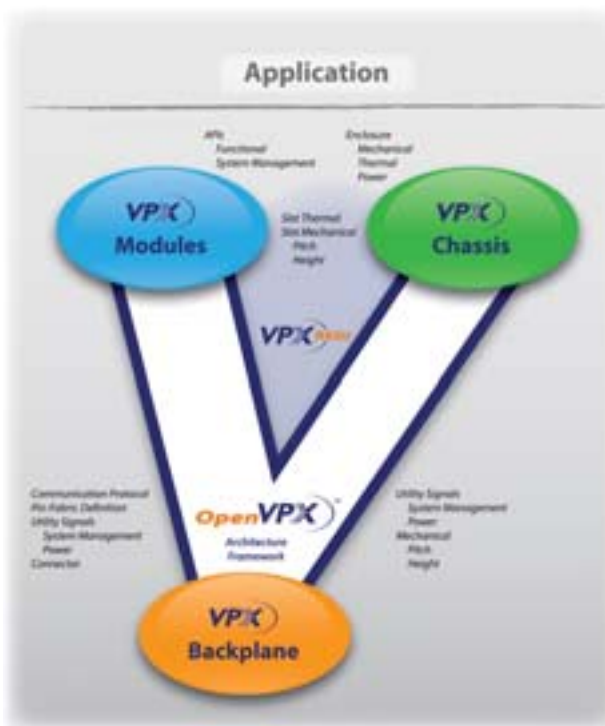
VPX is initially targeted at the military and aerospace markets but several other market segments have similar needs for critical embedded systems and are showing strong interest in VPX technology. These markets include: industrial, medical, communications, transportation, and research.

In a recent survey of the embedded computing industry conducted by VITA, 40% of the respondents indicated that they are designing new products with VPX now, and an additional 36% indicate that they intend to use VPX in future projects. This is an overwhelming vote of confidence for the technology. Suppliers are working hard to expand the product offerings, ensuring that designers will have the right commercially available products for their upcoming projects. Designers are very pleased with the performance, scalable and expandable architecture, high computational density, extended temperature, shock, and vibration capabilities, and choices of cooling schemes. They are looking forward to the long product life cycles that they have enjoyed with previous generations of technology from VITA members.

It appears that designers have plans to take advantage of the backplane topology flexibility built into the VPX specification. Designers are evenly spread between centralized (star) configurations, distributed switching (mesh or ring) configurations, and hybrid switching where numerous combinations exist, even some with parallel buses like VMEbus and PCI bus.

The VITA members working on VPX have over thirty additional working group projects underway to improve and complement the original VPX specification. New projects will surely be introduced to the working groups as the technology matures. These companies are fully committed to ensuring that VPX is the best solution for future critical embedded computing systems.

Ray Alderman  
Executive Director  
VITA



## FORWARD

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  - Forced Air-Cooled Enclosure
  - Two-Slot OpenVPX Development Platform
  - IPv4/IPv6 Gigabit Ethernet Switch



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### On the Cover

Initially targeted at the military and aerospace markets, OpenVPX will find new applications in a wide variety of critical embedded systems.

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# OpenVPX – From Concept to Specification

The OpenVPX Industry Working Group, a 28-company team founded by Mercury Computer Systems, collaborated with a common goal and accelerated the completion of a system architecture specification for open system COTS suppliers and integrators to specify, design, and build multi-vendor interoperable solutions.

## Timeline:

- **January 2009** – OpenVPX Specification effort by Mercury Computer Systems begins, based on VPX embedded community's need to accelerate multi-vendor interoperable solutions.
- **March 2009** – First open membership face-to-face meeting and call for membership.
- **Spring/Summer 2009** – Ongoing meetings, conference calls and discussions.
- **October 2009** – OpenVPX specification V1.0 completed and transition to VITA 65 working group.
- **January 2010** – VITA 65 Working group completed comment resolution, balloting and ratification of the specification.
- **June 2010** – ANSI VITA 65-2010 ratification of the OpenVPX System Architecture Specification.

Countless hours were spent with embedded community technical and business leaders (suppliers and integrators) to come up with a system-level architecture specification, dedicated to creating well-defined interoperability points for multi-vendor, 3U and 6U VPX integrated solutions. The inter-company marathon was a testament to what can be done when experts are dedicated to solving a significant industry issue for the good of the ultimate primary customer — the warfighters.

## So What?

If the following is important to your company or your customer, then OpenVPX should be important to you.

- Reduce TCO in integrated systems life cycle;
- Use of common language for simplified RFP generation;
- Choice of ecosystems to lower costs, get best-of-breed capabilities;
- Technology refresh possibilities with reduced obsolescence hurdles;
- Highly interoperable, multi-vendor integrated solutions development;
- Open standards, performance migration, and proliferation;
- Reduced risk to deployment for QRC programs;



- 1 GiGE, 10 GiGE, sRIO, PCIe gen 2.0 fabrics;
- Optimized SWaP smart processing via open architectures.

## VPX vs. OpenVPX

A board-level specification approach for VME bus technology was suitable due to its architectural simplicities, and it was logically brought forward as an approach for VPX specifications. While significant VITA standards work was in process, many technology users felt that the focus on the board-level specification(s) was not suitable for creating interoperable solutions for the complex application space that VPX technology is designed to serve. This includes a next generation of complex, rugged, integrated assets that consist of high-speed backplane fabrics and new processor technologies like multi-core x86 and GPGPUs.

In late 2008, VITA's Executive Director, Ray Alderman, and Mercury Computer's industry research determined a need for a new systems approach to specifying VPX. In January 2009 the Open VPX Industry Working Group was formed as the first step on the path forward to add system-level clarity to the specifications to accelerate the commercial benefits of VPX technology for integrated, multi-vendor systems. Available today, the ANSI-approved, OpenVPX systems architecture specification builds upon VPX technology (VITA 46 and dot specs) but does so from a top down, system engineering approach to specify interoperability points at the slot, module and backplane level.

## OpenVPX Taxonomy

The group created a common building block language to convey the key attributes of the OpenVPX specification. The definition of *Planes*, *Pipes* and *Profiles* were key taxonomy definitions allowing the user to specify a wide range of "building blocks" with a common set of intersections.

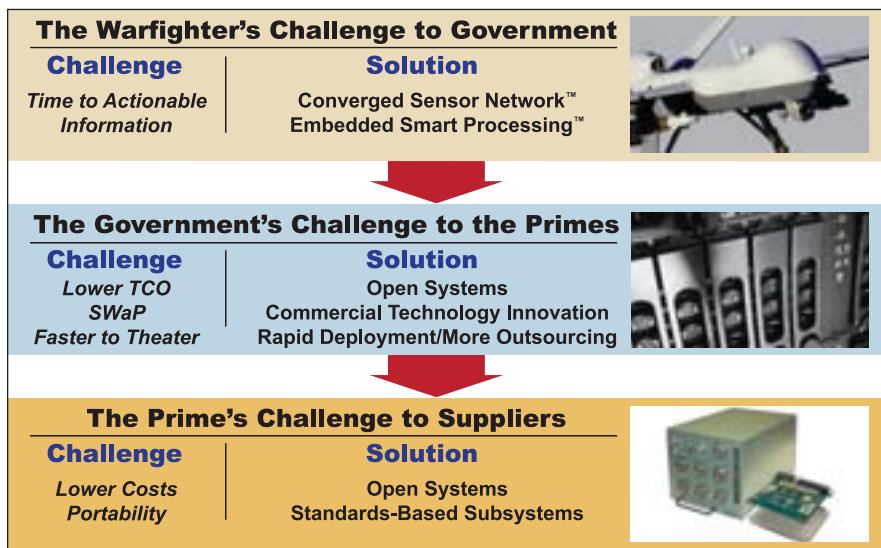


Figure 1. Cascading Challenges



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# » How do I reduce my risk when building my application solution around VPX/OpenVPX? «

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OpenVPX – From Concept to Specification

**Planes:** Segregated architecture boundaries for backplane and module connectivity

- Control Plane — dedicated to application software control traffic (1GE pipe).
- Data Plane — dedicated to application and external data traffic ( eg: 10GigE switch fabric).
- Expansion Plane — dedicated to communication between logical controlling system element and a separate, but logically adjunct, system resource (ex : PCIe lanes between multi-core and GPGPU modules).
- Management Plane — dedicated to supervision and management of hardware resources (eg. I2C).

• Utility Plane — dedicated to common systems services or utilities (Eg. SYSRESET, Power, Gnd, distribution, ref clocks).

**Pipes:** A collection of differential pairs assigned to a plane and used by slot profiles. Pipes are protocol- agnostic.

- Ultra Thin Pipe (UTP): 2 differential pairs (e.g. 1000BASE-KX Ethernet or 1X Serial RapidIO)
- Thin Pipe (TP): 4 differential pairs (e.g. 2x PCIe interfaces)
- Fat Pipe (FP): 8 differential pairs (e.g. 10GBASE-KX4, 4x PCIe)
- Double Fat Pipe (DFP):16 differential pairs (e.g. 8x PCIe interfaces)
- Quad fat Pipe (QFP): 32 differential pairs (e.g. 16x PCIe interfaces)

• Octal Fat Pipe (OFF): 64 differential pairs (e.g. 32x PCIe interfaces)

**Profiles:** The OpenVPX specification uses profiles for structure and hierarchy. Three Profile types exist: Slot, Module and Backplane.

- Slot Profile: Physical mapping of ports to a slot’s backplane connectors, using planes and pipes.
- Module Profile: Extends a slot profile by adding protocols, as well as thermal, power, and mechanical requirements.
- Backplane Profile: Physical backplane mapping of number of slot profiles and topology of slot interconnects.

**Backplane Topologies:** Different applications require different backplane

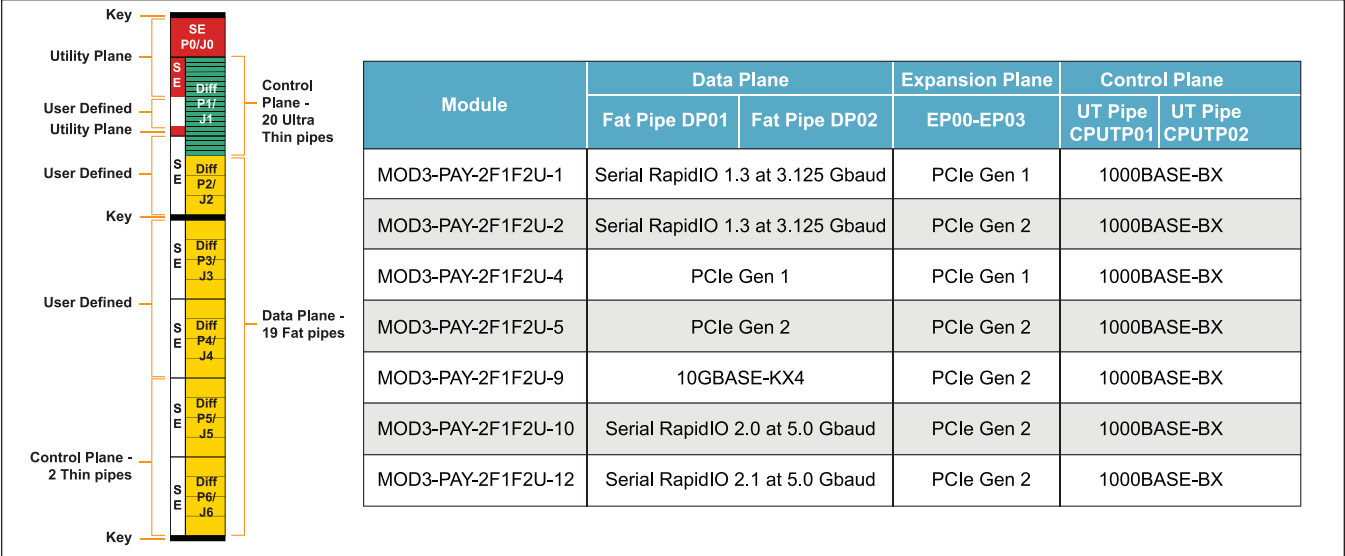


Figure 2. Determine the backplane profile and chassis topology required for the development chassis, and then select a standard OpenVPX reference chassis or create a custom configuration development chassis for design and integration.

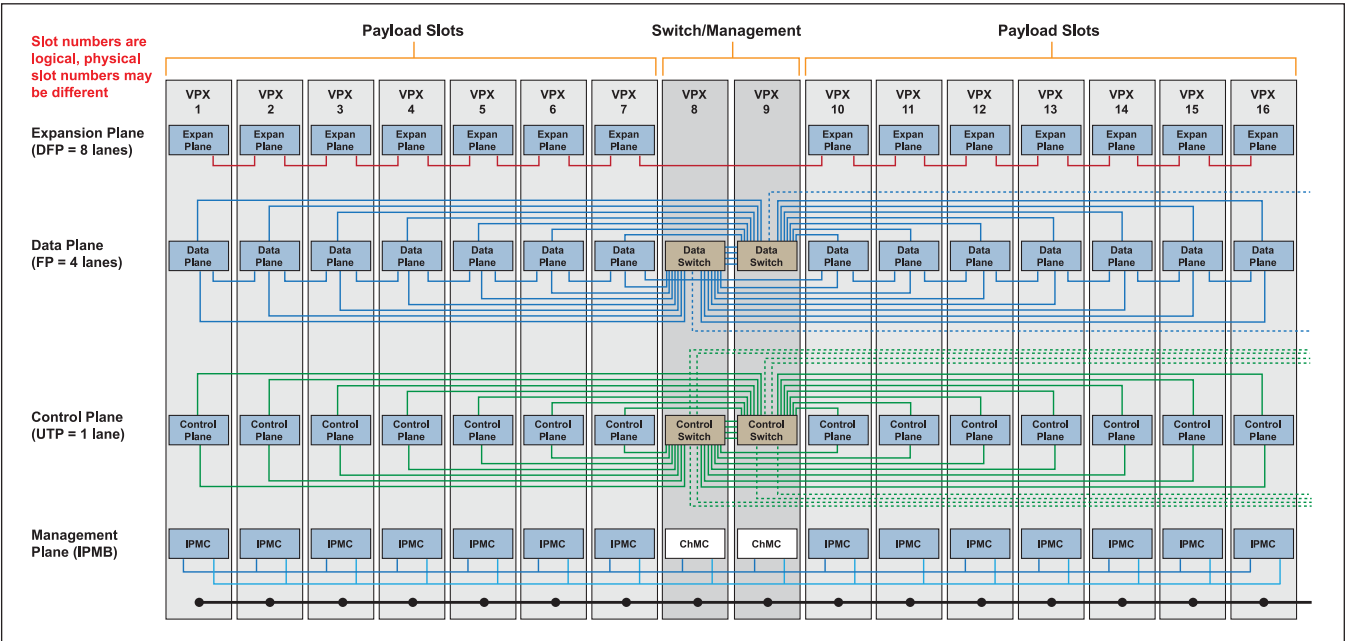


Figure 3. 16-Slot 6U Multi Plane Development Chassis Topology Wiring Diagram.

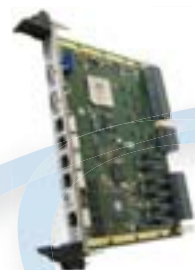


# Making Sense of

## OpenVPX™

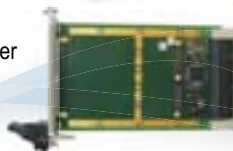
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## OpenVPX – From Concept to Specification

Task	(VITA 46) or Custom COTS Approach	Typical OpenVPX Savings	Comments
RFP generation for System elements	<ul style="list-style-type: none"> <li>Custom effort</li> <li>Interoperability holes</li> <li>No clear way to specify system requirements</li> </ul>	25-50% time	<ul style="list-style-type: none"> <li>OpenVPX assures common language and definitions</li> <li>Communications improved on requirements creation team</li> </ul>
System design	<ul style="list-style-type: none"> <li>Custom effort</li> <li>Significant error-prone backplane /chassis /module investigations</li> <li>Difficulty in getting agreement on needed design implementation</li> </ul>	50% time	<ul style="list-style-type: none"> <li>OpenVPX establishes well-defined choices</li> <li>System issues addressed</li> <li>Pinouts, placements, protocols defined in OpenVPX specification</li> </ul>
Development system readiness for integration	<ul style="list-style-type: none"> <li>Significant iterations with vendors before lock down</li> <li>Room for interpretation</li> </ul>	33% time or 50-60% time savings, if standard development chassis chosen	<ul style="list-style-type: none"> <li>OpenVPX assures common language and definitions</li> <li>Established ecosystem of standard backplane and chassis</li> </ul>
Multi-vendor hardware/system integration	<ul style="list-style-type: none"> <li>Rework cycles</li> <li>Finger pointing</li> <li>Cost, schedule, performance hits due to interoperability issues</li> </ul>	50% time	<ul style="list-style-type: none"> <li>OpenVPX published common language and specifications quickly resolves conflicts</li> </ul>
Risk to demonstrate readiness for initial flight-test	<ul style="list-style-type: none"> <li>High</li> <li>Reduced quality</li> <li>Technical, management, customer, team frustration</li> </ul>	50%+ risk reduction for integrated system goals with a clean architecture maintained	<ul style="list-style-type: none"> <li>OpenVPX reduces errors early in process</li> <li>Overall quality improves</li> <li>Overall QRC improves</li> </ul>

topologies. OpenVPX supports Centralized Switching, Distributed Switching, and Master/Slave Topologies.

- **Centralized Switching:** Uses dedicated switch modules in multiple types of switched configurations (e.g. Dual Star).
- **Distributed Switching:** Full or partial mesh switching. May require switch logic on each card for larger slot count chassis (e.g. 5 slot sRIO mesh).
- **Master-Slave:** Generally Master host SBC with Slave I/O cards connected by PCIe fabric. (e.g. SBC root complex connected to I/O cards via PCIe fabric.)

Using the OpenVPX specification taxonomy and the architectural building block language of connectivity, a system engineer or architect can now leverage the specification's content and rules for their unique application.

### OpenVPX Specification Decision Tree

The OpenVPX Specification (available now via ANSI and [www.vita.com](http://www.vita.com)) can be used in developing open architecture, high-performance, embedded hardware solutions. OpenVPX-compliant solutions provide a compatible hardware platform for open embedded OS and middleware layering. As a result, as the target application is developed, the OpenVPX specification can provide a performance migration path to using open middleware capabilities at the module, chassis and intra-chassis levels.

Here is a simple, high level "recipe" for using the OpenVPX specification for application development:

1. Establish application requirements to determine technology choice.
2. Decide on VPX technology — 3U or 6U form factor for SWaP requirements.
3. Is integrated multi-module, perhaps multi-vendor and /or system management enabled chassis solution required?
  - a. No — (standalone module only) Use VITA 46 specification(s) if desired.
  - b. Yes — Use OpenVPX specification. If yes, select **slot** and **module** payload profiles and, if switched architecture, **switch** module profiles that will allow assets to achieve (processing, throughput, management) application requirements.

Once this step in the solution development process has been reached, you have essentially constructed the architecture and topology of your development solution for application integration. You now have a clear template for design or for approaching suppliers for module, backplane and/or chassis outsourcing from an ever-growing ecosystem and cadre of OpenVPX suppliers.

### Achieving Significant Results and Benefits

The OpenVPX Open Systems architecture specification gives developers the tools to create complex OpenVPX technology applications for mitigating risk to Quick Response Capabilities (QRC) development programs and, ultimately, deployment. The above table identifies a typical set of tasks that may

be considered for a QRC VPX technology development program, noting estimated benefits anticipated from using the OpenVPX systems specification as a clear decision making guide to development. As an early thought leader and major contributor to the OpenVPX specification content, Mercury Computer was able to use these concepts to create and deploy a major prime QRC program using OpenVPX-compliant architectures in just 10 months. When systems developers with domain expertise and proposal writers become proficient with using the specification, similar types of risk reduction and development efficiencies may be expected.

### The Journey Continues

A path to OpenVPX V1.1 is being developed to create an efficient method to augment the specification with new profiles in support of technology and market changes. Also, recommendations for user-defined pins are in discussion, which hopefully will result in further VITA 65 specification definition, but still allow for innovation. As a result, the team is already looking forward to ensuring that OpenVPX will stay current and relevant as the world of fast-moving technology continues to evolve.

*This article was written by Bob Grochmal, Director, OpenVPX Program, Mercury Computer Systems, Inc. (Chelmsford, MA). For more information, contact Mr. Grochmal at [rgrochmal@mc.com](mailto:rgrochmal@mc.com), or visit <http://info.hotims.com/28057450>.*



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# Transitioning to OpenVPX for Next-Generation C4ISR Systems

VPX systems offer tremendous performance for the Mil/Aero market, including naval, airborne, and ground-based computing systems. The architecture provides an unprecedented combination of bandwidth, user IO, and rugged design, in both a 3U and 6U Eurocard format. The new OpenVPX initiative has opened up new definitions for VPX system interoperability, including defined module profiles, slot profiles, backplane & chassis configurations, secondary expansion fabrics and control planes, and higher speed fabric options.

## Command, Control, Communications, Computers, Intelligence, Surveillance and Reconnaissance (C4ISR)

C4ISR embedded computing systems have certain general needs, both today and continuing into the future. These include:

- **Mission-critical reliability** – For Mil/Aero applications, system failures can cost lives.
- **Higher bandwidth** – Weapon and intelligence gathering platforms are using more intensive digital signal processing for gathering, relaying, and processing data.
- **Rugged design** – Platforms need to survive the shock, vibration, and effects in aircraft, ground, and sea

based applications.

- **Stable architecture, less risk** – Platforms need to last many years, even decades. Vendor support is also critical.
- **Performance density** – As space restrictions get tighter, the system needs options for small form factors while retaining high performance.

VPX, and later OpenVPX, were collaboratively created within VITA (VME International Trade Association) by dozens of experts in the military/aerospace community. Based on the rugged Eurocard format like VME and CompactPCI, VPX comes in both 3U and 6U standard board sizes with typically 1.0" pitch (0.80" and 1.2" pitch are also possible). VPX uses a high-speed Multi-Gig connector and offers plenty of IO in a rugged, open standard architecture. With dozens of vendors and some backwards compatibility options to VME, the architecture is stable and will be supported for years to come.

## OpenVPX for System Interoperability

If there is any fault with VPX, it was made to be very flexible. This flexibility was beneficial for customized solutions, particularly for how high-speed IO is transported throughout the system. However, it was difficult, if not impossible, to be assured that a board from one vendor would work with one from

another vendor, along with a backplane from yet another party. Therefore, the OpenVPX initiative commenced in early 2009 with a goal of providing interoperability definitions for the VPX specification. The initiative was rolled into VITA as the VITA 65 specification, which was approved by ANSI in June 2010.

In short, OpenVPX provides definitions for backplane configurations, which are comprised of slot profiles into which various module profiles can be plugged. The module and slot profiles ensure that a vendor's VPX boards (modules) have pinouts that are interoperable within the VPX backplane slots. The backplane configuration tells the user which slot profiles are utilized, including information on the data rate, routing topology, and fabric used.

When it comes to backplane functionality, there is very little change. The new standard simply redefined two reserved P0/J0 signals Aux\_Clk (+/-) and added one P1/J1 single ended Utility signal of Maskable Reset and redefined the Res\_Bus signal to GDiscrete. The Aux\_Clk and GDiscrete pins were already bussed anyway, so the change is minimal. Also, the SysCon signal is now configurable.

Let's take a look at a standard 6U VPX 5-slot Mesh backplane and compare it to an OpenVPX version. Figure 1a shows a 6U 5-slot VPX backplane and 1b shows a side-view diagram of how the J0-J6 connectors are used.

The standard VPX version has pinout charts for P0 and P1 sections with the P2-P6 as "undefined". Although the P0 and P1 sections have defined pinouts, there are no details in VPX as to the kind of signals such as thin pipes, fat pipes, or ultra thin pipes. Also, the details of the utility plane are not as clear.

In the OpenVPX version of the same backplane, Figure 2 shows the payload slot profile. It provides more information for the data plane section (in yellow), which in this case defines 4 fat pipe lanes. Also, the utility plane sections are clearer. Although this backplane does not have a control plane, if it had one we'd also see this in the payload slot profile, along with the type of signal (thin pipes are commonly used for the control plane).

The Slot Profile that is referenced in Figure 2 gives us some details on the card plugging into the slot. For example, the slot profile number SLT6 says it's a 6U slot

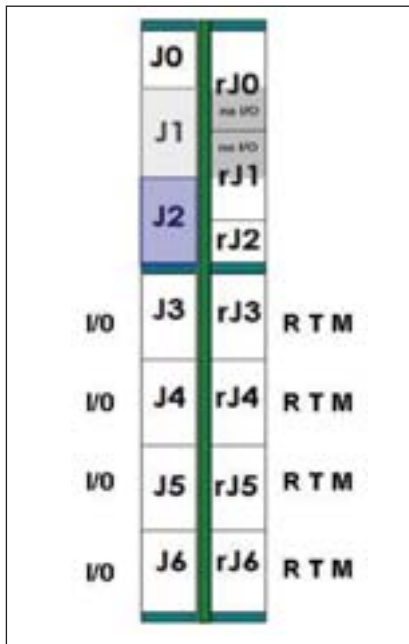
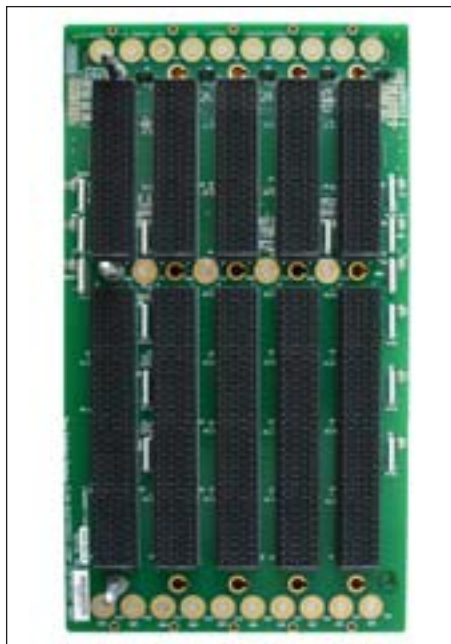


Figure 1. Figure 1a shows a standard 6U 5-slot VPX backplane and 1b shows a simple side-view diagram of how the J0-J6 connectors are used.





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Think of this reference book as Cliffs Notes for VPX and OpenVPX. It's that comprehensive and easy to read. It covers all the key topics, including the VITA 46 (VPX) specification, VITA 48 (VPX REDI), and VITA 65 (OpenVPX). It covers the history and rationale for VPX, its underlying principles and features, describes in detail important technical information, and illustrates the content with over 50 diagrams, charts and photos. Ordering one is a no-brainer.

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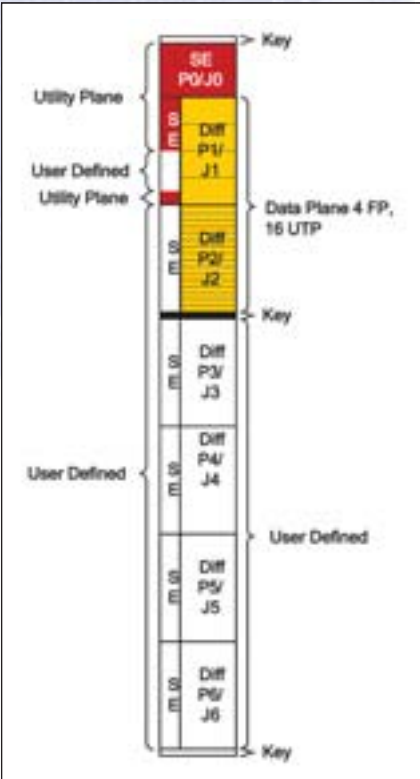


Figure 2. A Slot Profile of an OpenVPX (VITA 65 compliant) version of the 6U 5-slot backplane. The profile provides more details on the data signals, utility plane, and more.

profile (a 6U board), the PER says it's a peripheral slot, 4F means it has 4 fat pipes and the 10.3.1 is where you can find details on this slot profile in the VITA 65 specification. For OpenVPX, fat pipes have 4 links (4 Tx pairs + 4 Rx pairs), thin pipes have 2 links, and ultra thin pipes have one link. The wider bands, like fat pipes, are typically used in the data plane, while the control plane will often have the thin pipe or ultra thin-pipe signals. Slot types are comprised of peripheral slots, payload slots, switch slots, or bridge slots. The backplane profile of the backplane also provides more information. For example, this 6U 5-slot's profile is

BKP6-DIS05-11.2.16-1. The BKP6 tells us it's a 6U backplane profile. DIS05 means it's a distributed (like a mesh or ring) architecture and has 5 slots. The 11.2.16 is the section of the specification where you can find details on this backplane profile. The "-1" tells us the data rate is 3.125 Gbps (-2 means 5 Gbps and -3 means 6.250 Gbps). The backplane profile chart in Figure 3 shows the profile name, the pitch, the corresponding slot profile for the backplane, the control plane data rate (if applicable) and the data rate of the backplane. The slot type (like DIS05) section of the profile name is an important part of

Profile name	Mechanical		Slot Profiles and Section	Channel Gbaud Rate	
	Pitch (in)	RTM Conn		Control Plane	Data Plane
BKP6-DIS05-11.2.16-1	1.0	VITA 46.10	SLT6-PAY-4F-10.2.4	1.25	3.125
BKP6-DIS05-11.2.16-2	1.0	VITA 46.10	SLT6-PAY-4F2T-10.2.4	1.25	5.0
BKP6-DIS05-11.2.16-3	1.0	VITA 46.10	SLT6-PAY-4F2T-10.2.4	1.25	6.25

Figure 3. The Backplane Profile Chart tells us which OpenVPX Slot Profile(s) is used, the pitch, and data rate of the backplane.

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## Transitioning to OpenVPX

the description. The main fabric topologies are CEN for centralized, DIS for distributed, and HYB for hybrid. "Centralized" means it has a centralized switch slot and the routing could be similar to a Star topology. The DIS and CEN configurations typically have payload and switch slot types. The HYB will typically also define peripheral, bridge, and bus slot types like "VME" to account for connections to the legacy bus slots. The bridge slot does not mean an active bridge board (like a cPCI Bridge) is being used. Rather, it

just refers to the fact that this VPX slot also has pinouts defined for the parallel bus (like VME).

### Future Designs for VPX/OpenVPX

There are some interesting configurations coming up in OpenVPX. They include special connections for optical connectors and another version for a RF connector interface. VITA 67 is underway to add RF connectors to the OpenVPX backplanes. Figure 4 shows the new gold connectors on a backplane.

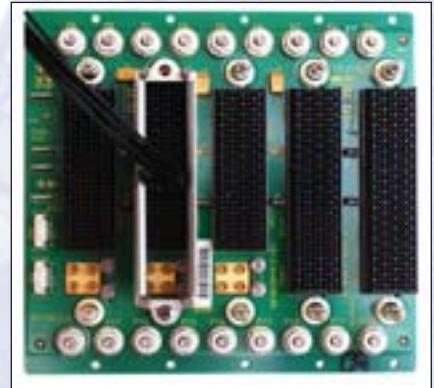
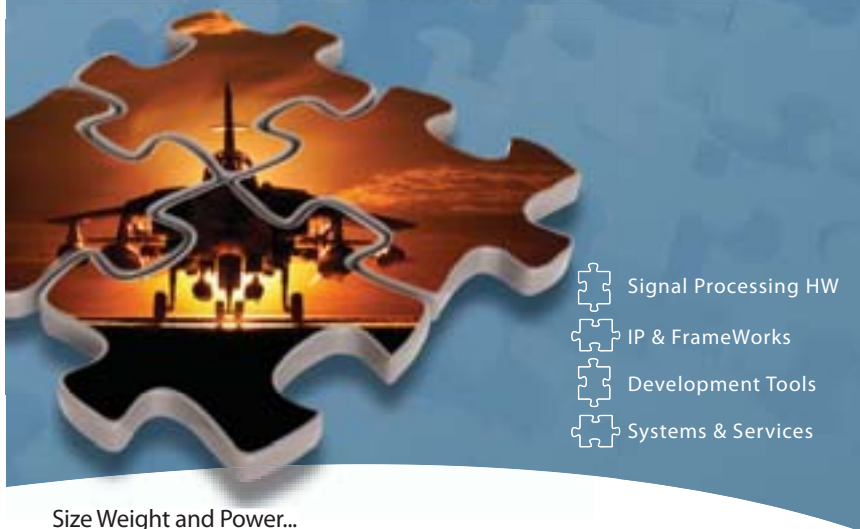


Figure 4. This photo shows two upcoming solutions in one. The gold connectors are for RF signals per the VITA 67 specification underway. Also shown is a VPX cabling solution with a shroud to secure the cables that clip into the backplane.

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Another very compelling new solution for VPX is cabling systems. Compliant to the latest VITA 46 specifications, the cabling system can be used for IO to bulk-head connectors, slot-to-slot connections, and out-of-band communication. The cabling system can also be used for system development. Figure 4 also shows an example of these cables plugged into a VPX backplane. The direct cabling system also has front-plug versions, which allow testing across the backplane or full interconnect path. The metal shroud can be used in deployable systems to securely hold the cables in place and satisfy MIL-STD-810E and 901D for shock and vibration.

There are several reasons to use a cabling system in a deployed VPX platform. Many applications such as ATRs (air transport racks), may not have RTM (rear transition module) options. In some cases, the signal speeds through the RTM are not enough. In other designs, the system cannot afford to lose a slot of space to an IO slot. The VPX cabling system provides a rugged and robust alternative with a high-speed connection that is plugged directly into the MultiGig connector in single or multi-wafer formats.

OpenVPX provides definitions for VPX backplanes, modules, and chassis to ensure that the products are interoperable. The backplane configurations have been defined to show the collection of slot profiles it entails, including information on the data rate, routing topology, and fabric used. Exciting VPX/OpenVPX products have emerged that offer the performance solutions required in C4ISR systems.

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# Putting OpenVPX To Work

Before the advent of OpenVPX, designers of embedded systems took advantage of the extreme connectivity offered by VPX (VITA 46), but were faced with a virtually unlimited number of possible implementations. Specific choices for the control and data channel assignments for each slot, the backplane connectivity, and serial fabrics were often made somewhat arbitrarily to suit the particular needs of the current system. Although following the general framework of VITA 46, each system tended to be so unique that the boards and backplanes designed for one system were seldom usable in other systems, even from the same vendor.

Now, OpenVPX (VITA 65) provides an effective taxonomy for describing VPX components, and also defines numerous “profiles” for boards, slots and backplanes that detail specific configurations of channels, interconnections, and fabrics. Instead of starting from scratch each time, designers can browse through

these standardized profiles to find one that satisfies the objectives of each new system. By narrowing the field of configurations, these profiles boost reusability and interoperability between vendors.

## Beamforming Principles

A multichannel software radio beamforming receiver system is presented as an example that illustrates how the OpenVPX system design process works. Principles from this example can be easily applied to other systems.

Beamforming is extensively used in communications, radar, direction finding, countermeasures, weapons systems, oil and mineral exploration, and medical imaging and treatment. In essence, beamforming utilizes multiple sensors to achieve directionality of the sensor array, and also to improve the signal quality and reception range.

Beamforming achieves these benefits by judiciously adjusting the phase shift and gain of each sensor so that, when

the adjusted sensor signals are combined, they add constructively. For receivers, the combination is performed by summing the adjusted signals from each sensor. For transmitters, each sensor delivers a signal that adds constructively at the destination.

## Defining System Requirements

The sensors in a software radio receiver system for beam forming are antennas arranged in a linear or two-dimensional array. The term “software” in software radio refers to the programmability of the digital signal processing functions including the digital down conversion, phase shifting, gain adjustments, summation of the received channels, and then the ultimate demodulation, decoding, and/or decryption of the acquired signal.

The example system requires sixteen antennas, each followed by an RF stage to amplify and down convert the radio frequency signal to an intermediate frequency (IF) analog signal so it can be digitized by an A/D converter. These sixteen IF signals are supplied as inputs to the system.

Each IF signal has a bandwidth of 20 MHz and is centered at 70 MHz. After A/D conversion, all sixteen channels are down converted to baseband and beamformed using gain and phase shift parameters to comply with operational objectives. The final beamformed sum is delivered as a baseband signal to a remote system control processor PC for additional processing, forwarding, or storage.

The system must operate in a limited space avionics equipment bay and must comply with typical shock, vibration, temperature, altitude, humidity, flight safety, power consumption, power supply, and EMC/EMI standards.

## Choosing the OpenVPX Payload Module for Beamforming

Since industry standard chassis are available in both 3U and 6U sizes, and both are well defined for OpenVPX, the small avionics bay requirement favors the 3U style. The next tasks are to select the appropriate 3U software radio and processor modules (boards) to perform the beamforming, define the required connections between the modules, select a 3U backplane to support those inter-

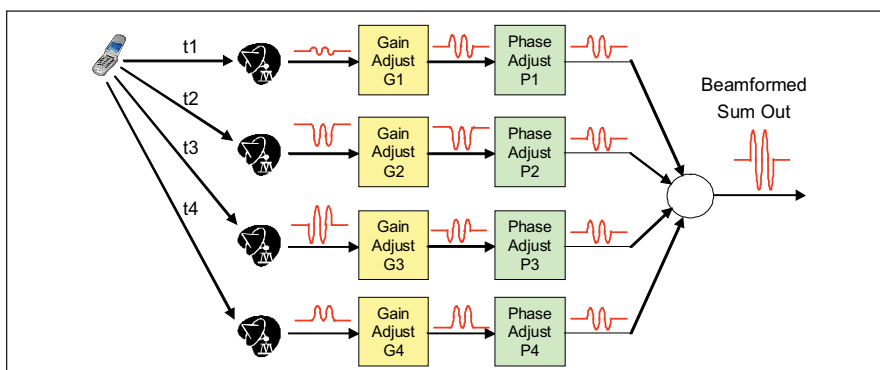


Figure 1. Beamforming adjusts phase and gain of signals from each antenna in an array to compensate for different delays ( $t_n$ ), so that signals arriving from a particular angle relative to the array add constructively when combined in the summer.

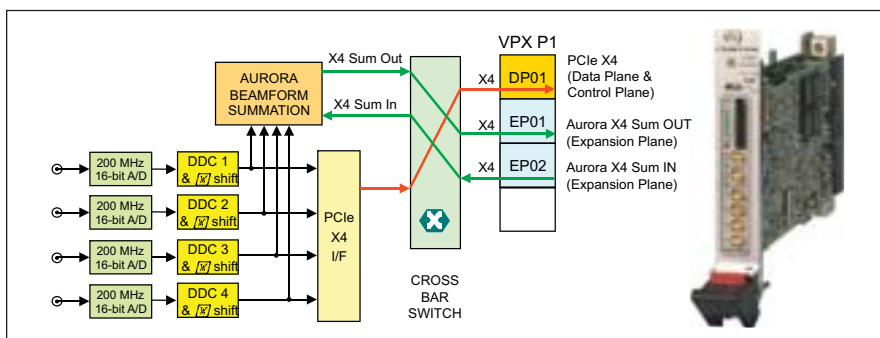


Figure 2. Model 5353 3U VPX Beamformer Module with four A/Ds, four DDCs, X4 PCIe interface, phase shifters and summation engine for beamforming.



## Putting OpenVPX To Work

connections, a chassis to meet the physical and environmental requirements, and a link between the chassis and the remote system control processor PC.

For example, Pentek's Model 5353 Software Radio Beamformer is a 3U OpenVPX module featuring four 200 MHz 16-bit A/D converters and two Virtex-5 FPGAs, one for signal processing and a second one for the PCI interface. Inside the first FPGA are interfaces to the four A/D converters, four digital downconverters (DDCs) with programmable phase shift and gain, and four power meters at each DDC output. A simplified block diagram of the 5353 is shown in Figure 2.

The Model 5353 also includes a summation block that adds the DDC outputs for a four-channel beamforming sum. This block also accepts a propagated sum in signal from another module and generates a propagated sum signal out to the next module. The sum in/sum out signals use two X4 Aurora gigabit serial links connected to the VPX P1 backplane connector, each capable of moving data at 1.25 GB/sec peak.

To support the 20 MHz IF channel bandwidth with a 25% filter margin, the DDC outputs deliver complex 16-bit I+Q samples at 25 MHz, or 100 MB/sec. The propagated sum in/sum out signals also operate at 100 MB/sec and are thus easily handled by the 1.25 GB/sec X4 Aurora links.

The 5353 system interface for control and data is an X4 PCIe port, also connected to P1. Bandwidth requirements for the control and data port are dominated by delivery of the final beamformed sum out to the control processor. This 100 MB/sec stream falls well within the 2 GB/sec peak rate of the X4 PCIe port when operating in Gen 2 mode.

A programmable, fabric-transparent crossbar switch allows free assignment of the two X4 Aurora ports and the X4 PCIe port, in any combination, to the four X4 fat pipes of P1. This flexibility allows the 5353 to accommodate various OpenVPX slot profiles and backplanes.

To accommodate 16 antennas, a total of four 4-channel 5353 modules are required. Since the summation chain requires the same data rate as each DDC, the two sum ports must simultaneously handle 100 MB/sec each. This class of signals falls under the definition of expansion plane in the OpenVPX specification.

The X4 PCIe interface for handling the data initialization, delivery of beamforming parameters is described as the control plane under OpenVPX. Final delivery of the beamformed result to the

system control processor is best classified as the data plane under OpenVPX.

### Choosing the OpenVPX Backplane

OpenVPX backplanes use many different topologies named after the geometry of their interconnections, including mesh, star, leaf, and ring. Most include slots for switch modules to support reconfigurable inter-board connections, while some simply rely on dedicated wiring between the slots.

After reviewing the 3U OpenVPX backplane choices in the standard, the most appropriate for our system is the 6-Slot backplane profile BKP3-CEN06-15.2.2-1, which has five payload slots and one switch slot as shown in Figure 3.

The expansion plane fat pipes join adja-

cent payload slots 1 through 5 to support the sum in and sum out chaining ports between 5353 modules. One data plane fat pipe from each payload slot to the switch slot 6 supports the four X4 PCIe links we need to the control processor.

This backplane defines specific slot profiles for the two types of slots. Slots 1 through 5 use the payload slot profile SLT3-PAY-1F2F2U-14.2.2 shown in the upper right section of Figure 3. To see if we can use the Model 5353 in the payload slots, we must verify that the Model 5353 has a module profile compatible with this slot profile.

It is important to note that the backplane profiles and slot profiles do not specify any fabric or protocol for the connections. However, the backplane profile does speci-

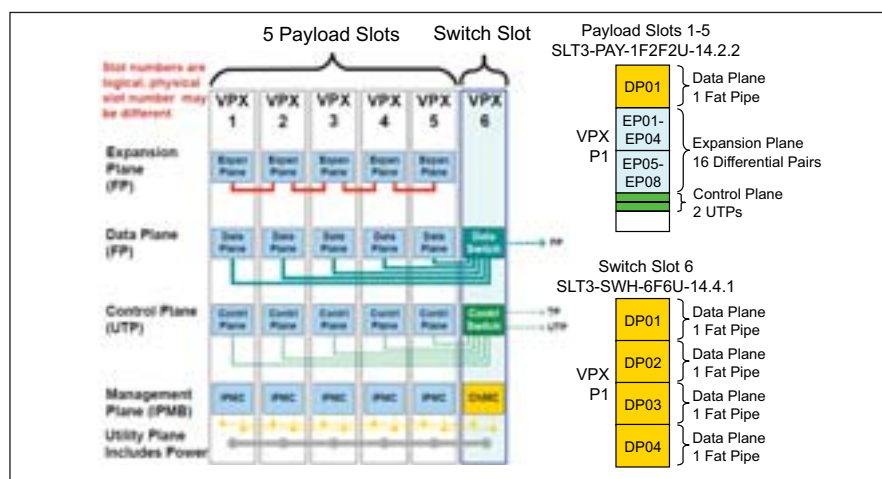


Figure 3. OpenVPX 3U 6-Slot Backplane BKP3-CEN06-15.2.2-n showing definition for the payload slot profiles and switch slot profiles.

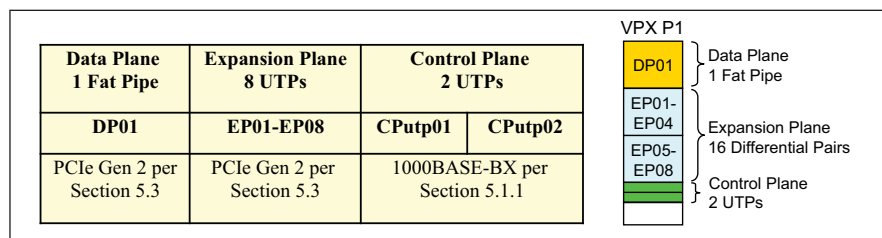


Figure 4. Fabric definitions listed for the module Profile MOD3-PAY-1F2F2U-16.2.2-4 (for the model 5353) are completely compatible with the VPX P1 connections for payload slot profile SLT3-PAY-1F2F2U-14.2.2, defined for backplane profile BKP3-CEN06-15.2.2-1.

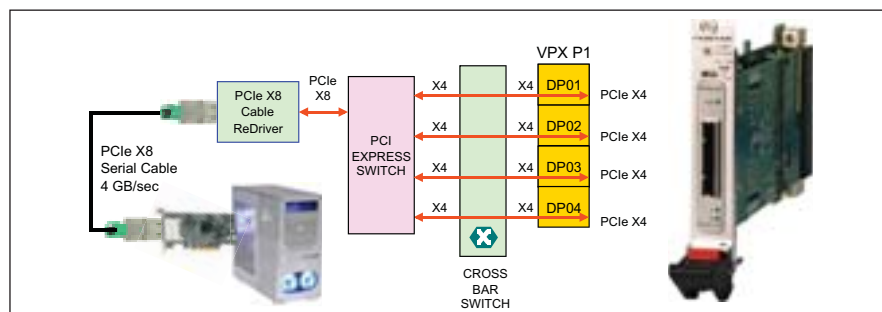


Figure 5. Model 5308 3U VPX PCIe X8 Serial Cable Adapter with ReDriver, PCIe switch and crossbar switch. Also shown are the X8 PCIe cable, PC host adapter board, and host PC.



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fy the maximum baud rate for each gigabit serial pipe. This scheme allows a wide variety of modules to be used in a given backplane slot, each with its own particular fabric and baud rate. Of course, the baud rate of each pipe of the module must be equal to or less than the maximum baud rate specified in the backplane profile.

Because of its programmable crossbar switch, the Model 5353 can be configured to meet the module profile MOD3-PAY-1F2F2U-16.2.2-4, which is compatible with the slot profile SLT3-PAY-1F2F2U-14.2.2. This module profile defines data, expansion and control plane fabric connections and baud rates. The backplane profile BKP3-CEN06-15.2.2-1 defines a single fat pipe (X4) on the DP01 data plane for PCIe Gen 2 that corresponds directly to the PCIe interface as shown in Figure 4.

The eight expansion plane ultra thin pipes, EP01 through EP08, are also defined as PCIe Gen 2, capable of operating at baud rates of 5 GHz. We will organize these eight pipes as two fat pipes for the two X4 Aurora ports for sum in and sum out, which need to operate at only 3.125 GHz. The two control plane ports, CPutp01 and CPutp02, are not implemented on the 5353.

### Choosing the OpenVPX Switch/Interface Module

The selected backplane also has a switch slot with profile SLT3-SWH-6F6U-

14.4.1, whose VPX P1 connections are shown in the bottom right section of Figure 3. The four data plane fat pipes shown (DP01 — DP04) connect to payload slot fat pipes DP01 on slots 1 through 4.

Now we need to find a compatible switch module that can plug into slot 6 and connect these four PCIe links to the remote system control processor. Pentek's Model 5308 PCIe Cable Adapter is a 3U VPX switch module with a front panel X8 PCIe cable connector defined by the PCI-SIG PCI Express® External Cabling 1.0 Specification. Compatible PCIe host adapters are available for many different systems including PCIe cards for desktop PCs as well as avionics cockpit computers.

The 5308 features a PCIe switch that supports flexible lane bonding so that a single X4 or X8 PCIe port from the control processor PC can be split into four X4 PCIe ports to four individual PCIe endpoints. The fabric-transparent crossbar switch joins these four X4 ports to the VPX1 P1 backplane connector, fully compatible with OpenVPX module profile MOD3-SWH-4F-16.4.5-2 shown in Figure 6.

Inspection reveals that this module profile is fully compatible with the four VPX P1 fat pipes on the slot profile SLT3-SWH-6F6U-14.4.1. Further, the baud rate specified for the backplane profile BKP3-CEN06-15.2.2-1 supports the PCIe Gen 2 with baud rates up to 5 GHz.

The final beamforming system is shown in Figure 7, with simplified block diagrams of the four Model 5353 Beamformers and the 5308 PCIe Cable Adapter. All of the required gigabit serial links for Aurora expansion plane and PCIe data and control planes are connected by the backplane wiring.

The chart in the diagram shows the OpenVPX profiles for the backplane, the slots, and the modules that plug into those slots. Each profile is described in full detail in the specification and the system designer must ensure that the profiles are compatible.

This process of matching module profiles, slot profiles, and backplane profiles for a particular application is the key to successful system configuration under OpenVPX. Not all of the resources of each profile need to be fully implemented or utilized if the needs of the application are satisfied.

Finally, the chassis profile needs to be defined based on the environmental and physical constraints of the system. OpenVPX does not yet have specific chassis profiles defined, but it offers a complete system for specifying the size, type (rack mount, tower, etc), slot count, primary power, cooling, backplane power, and the profile name.

### Summary

OpenVPX presents a formal, well-organized system for defining all components in VPX systems, and the efforts of the working group should be applauded. Many of the figures and all of the profiles in this article were derived from the full OpenVPX VITA 65 specification, which is available from the VITA website ([www.vita.com](http://www.vita.com)), and is definitely a worthwhile and important reference document.

A good metric for the significance of a new standard is how actively new extensions are proposed to embrace new options and new technology. As promising evidence, even before final ratification, new initiatives like VITA 66 and VITA 67 were proposed, adding both optical and RF I/O capabilities. As OpenVPX is applied to an increasing number of application systems, the need for future evolutionary capabilities will emerge. All signs point to growing adoption of OpenVPX for new programs by both the embedded systems industry and its customers.

*This article was written by Rodger Hosking, Vice President, Pentek, Inc. (Saddle River, NJ). For more information, contact Mr. Hosking at [Rodger@pentek.com](mailto:Rodger@pentek.com), or visit <http://info.hotims.com/28057-452>.*

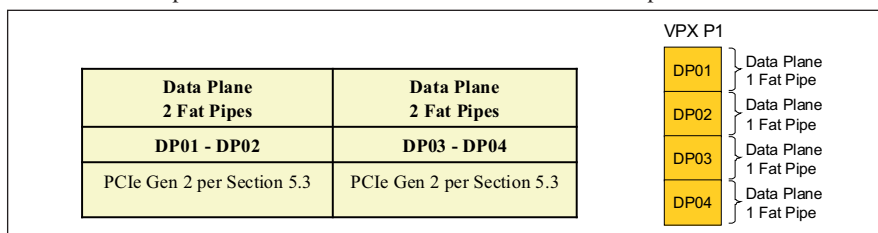


Figure 6. Fabric definitions listed for the module Profile MOD3-SWH-4F-16.4.5-2 (for the model 5308) are data rate compatible with the VPX P1 connections for payload slot profile SLT3-SWH-6F6U-14.4.1, defined for backplane profile BKP3-CEN06-15.2.2-1.

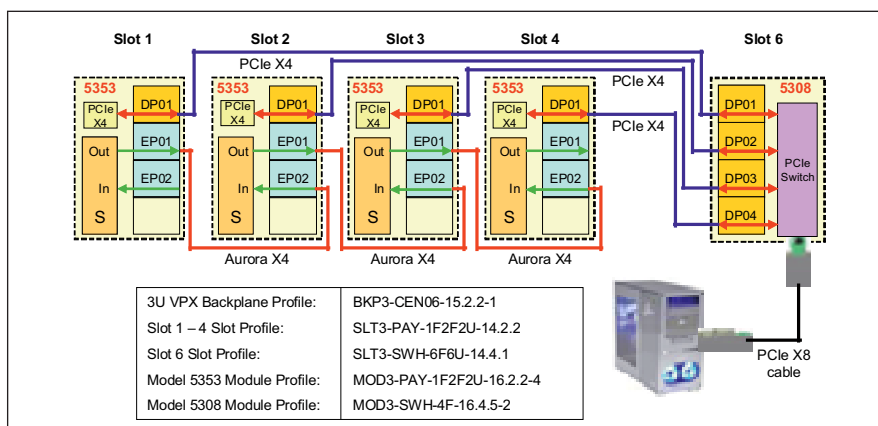


Figure 7. Complete OpenVPX beamforming system showing four 5353's with Aurora X4 sum in/out links (red), and PCIe X4 links (blue) connected to one 5308 with PCIe X8 cable link to the PC.



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## 6U OpenVPX Radar System Upgrade

Available in both air- and conduction-cooled configurations, the Ensemble™ 6000 Series OpenVPX HCD6410 High Compute Density Module from Mercury Computer Systems (Chelmsford, MA) combines eight high-performance Power Architecture processor cores with various I/O capabilities and the scalable serial RapidIO interconnect. The HCD6410 also features the MultiCore Plus® software infrastructure, which allows ease of portability in an open software development environment.

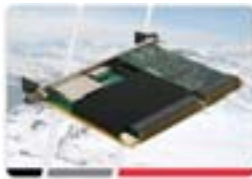
**For Free Info Visit <http://info.hotims.com/28057-455>**



## OpenVPX/VITA-65 Serial RapidIO® GEN-2 Switch

Curtiss-Wright Controls Embedded Computing (Ottawa, Ontario, Canada) has introduced the OpenVPX™/VITA-65 compliant VPX6-6902 Serial RapidIO® (SRIO) switch card. This rugged 6U VPX board, available in both air- and conduction-cooled versions, combines Ethernet and SRIO switching in a single slot for management, control, and dataplane switching in high performance embedded military systems. Supporting both Gen-1 SRIO (1.25, 2.5, 3.125 Gbaud) and Gen-2 SRIO (5.0, 6.25 Gbaud), the VPX6-6902 enables systems integrators to quickly and easily architect small to large high-performance systems that adhere to the VITA-65 OpenVPX™ systems specification.

**For Free Info Visit <http://info.hotims.com/28057-456>**



## 6U OpenVPX Rugged Single Board Computer

GE Intelligent Platforms (Charlottesville, VA) has announced the SBC622 rugged 6U OpenVPX-compliant single board computer. At 2.53GHz, the SBC622's Intel Core i7 processor is 30% faster than its predecessor, with up to 8 GBytes of soldered DDR3 SDRAM with ECC and a high bandwidth 10 Gigabit Ethernet I/O fabric subsystem. Customer flexibility to configure the SBC622 according to the precise requirements of the application is delivered via two onboard PCI-X® PMC/XMC mezzanine expansion sites. Provision for a higher degree of failsafe operation is delivered through the SBC622's onboard BIOS flash which can be optionally backed with a second flash device.

**For Free Info Visit <http://info.hotims.com/28057-457>**



## 6U VPX Load Board

Elma Bustronic Corporation (Fremont, CA) has introduced a new 6U VPX Load Board that helps confirm the chassis meets the VITA 46/48 power specifications for VPX and aids in locating hot spots within the enclosure. The 6U VPX load card features a microcontroller-based stepped load control to 100W maximum. Go-No-Go indicators are present for 3.3V, 5V, 12V, +12V\_Aux, -12V\_Aux and 3.3V\_Aux. The rotary switch selects the voltage setting while pushing the ON switch will cycle between different power levels shown on the LED display. The set load power levels are saved in EEPROM. Other features include a power reset button (to minimum level) and a SYSRESET signal on the two test point outputs.

**For Free Info Visit <http://info.hotims.com/28057-458>**



## Forced Air-Cooled Enclosure

Extreme Engineering Solutions (X-ES) (Middleton, WI) is now shipping the XPand4200, a sub-½ ATR, forced air-cooled enclosure for conduction-cooled modules. The system measures 4.88" (W) × 6.0" (H) × 13.5" (D) and weighs 8.8 pounds. The XPand4200 has an optional removable memory module attachment that supports the XPort6191 Solid State Disk (SSD) removable storage module, with 64 GB of storage capacity. With the memory module attachment the height increases to 7.62" and the weight to 11.1 pounds. Up to six conduction-cooled, 0.8" pitch 3U VPX, 3U cPCI, or power supply modules can be configured into the XPand4200. Additionally, the XPand4200 can be configured to meet custom I/O requirements with conduction-cooled PMC / XMC modules available from X-ES or third parties.

**For Free Info Visit <http://info.hotims.com/28057-459>**



## Two-Slot OpenVPX Development Platform

Elma Electronic Systems Division (Fremont, CA) has released a new two-slot VPX/OpenVPX test and development platform that accommodates both 3U and 6U boards via a shelf divider. The new E-Frame Series enables developers to power up one or more VPX blades under test and interconnect the J1 fabric connections to emulate the user's application. The use of a standard VPX RTM (rear transition module) plugged into the back provides access to the J0, J2, J3, J4, J5 and J6 connectors, while simultaneously accessing high-speed signals in the J1 connector, routed out the side of the backplane. Each slot's J1 "A" channel is broken out into 16 SMA connectors and the "B", "C" and "D" channels into four SATA2 cable headers (12 total per slot).

**For Free Info Visit <http://info.hotims.com/28057-460>**



## IPv4/IPv6 Gigabit Ethernet Switch

The new Kontron (Poway, CA) Gigabit Ethernet Switch VX3910 offers 3U VPX (VITA 46.x) and OpenVPX™ (VITA 65) platforms enterprise-class switching functionality with a total of 28 Gigabit Ethernet ports and advanced management features. The non-blocking fully managed L2/L3 Gigabit switch, Kontron VX3910, with its 20x Gigabit ports to the backplane, offers the highest port density for the implementation of various network topologies in 3U appliances. Four additional 2.5-Gigabit ports to the backplane simplify a redundant system architecture with multiple switches with no single point of failure. The four 1000 Base-T uplinks on the front panel, one dedicated for out-of-band management, expand the range to a total of 28 ports. The new Kontron Gigabit Ethernet Switch VX3910 is available in an air-cooled version for ambient temperatures from 0°C to +55°C and in a rugged conduction-cooled version for the extended temperature range from -40°C to + 85°C.

**For Free Info Visit <http://info.hotims.com/28057-462>**



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## Enabling Interoperability in High-Performance Embedded Applications - An OpenVPX System Specification Primer

With the advent of high-speed serial fabrics, the VME Parallel Bus proved insufficient for the needs of higher performance embedded systems. VPX, also known as VITA 46, is the follow-on to the VME Specification for the next generation of high-speed interconnects for harsh environments. While advancing the state of the technology, VPX provides backwards compatibility to traditional VMEbus through the use of specialized bridges.

**Curtiss-Wright Controls Embedded Computing**

<http://www.techbriefs.com/wp/8360>



## OpenVPX Backplane Profiles: Making Sense of System Interoperability For VPX

OpenVPX has opened up new definitions for VPX backplanes and systems. This includes defined Module Profiles, Slot Profiles, backplane & chassis configurations, secondary expansion fabrics and control planes, and higher speed fabric options. Elma Bustronic will provide some clarity for the new definitions and what they entail. We'll provide an overview of the various elements involved, and include a couple of potential backplane configurations. The paper will include diagrams on module and slot profile examples, illustrate signal changes for existing VPX products, and configuration examples.

**Elma Bustronic**

<http://www.techbriefs.com/wp/8361>



## OpenVPX Enables New Levels of High-Performance Video Technology Applications

With powerful and mature video technology applications available nowadays, two typical bottlenecks still exist in actual systems: data throughput in the gigabit/s range to support high-definition video standards, and system component interoperability due to the inner complexity of high-performance video applications. OpenVPX can reliably address both issues.

**Creative Electronic Systems (CES)**

<http://www.techbriefs.com/wp/8368>



## Enabling High-Speed Data Rates in Connectors for Commercial Aerospace and Defense Applications

A new high-speed connector system for aerospace and defense applications builds on industry-proven technology to achieve new levels of ruggedness. By combining the designs of cutting-edge high-speed connectors with proven MIL-SPEC contacts, the new Fortis Zc connector meets the demands of emerging military applications by enabling data rates of 10 Gb/s+ while performing in military-level vibration and shock conditions.

**Tyco Electronics**

<http://www.techbriefs.com/wp/8362>



## The Inner Workings of Solid State Flash: SLC versus MLC

Because all solid state flash products are not created equal and flash storage is finding its way into more and more embedded computing applications, system designers should understand the critical tradeoffs between competing technologies when evaluating flash products. Two well-known flash storage technologies, Single Level Cell (SLC) and Multi Level Cell (MLC), offer distinct advantages depending upon a user's needs.

**Elma Electronic**

<http://www.techbriefs.com/wp/8363>



## VPX: A Rugged Fabric Architecture for the 21st Century

The VMEbus architecture has served military embedded computing applications well for over a quarter of a century. Increasingly demanding applications, coupled with new technologies such as serial switched fabrics, meant that a new derivative - VITA 46, now VPX - was required that leveraged many of the familiar characteristics of the VMEbus architecture but brought new levels of performance. While introducing some elements of incompatibility with what has gone before, VPX brings substantial improvements in price/performance.

**GE Intelligent Platforms**

<http://www.techbriefs.com/wp/8365>



## Deploying Ruggedized Systems in Unmanned Military Vehicles for Advanced Air-Sea-Land Applications

Over the past decade, military platforms of all types and sizes have seen a dramatic increase in the use of sophisticated onboard electronic systems. This growing reliance on small embedded, rugged computers and complex high-speed I/O requirements for "mission computing" provides a wide range of real-time applications to support both reconnaissance and war-fighting activities on land, in the air and at sea.

**Kontron**

<http://www.techbriefs.com/wp/8364>



## The Advantages of OpenVPX Open Standard for VPX COTS Equipment Suppliers and System Integrators

The OpenVPX specification was created with a top-down, systems-level view of performance and interoperability. Addressing the architectural issues required to define, implement, and deploy VPX-based systems from a broad choice of interoperable, COTS hardware building blocks from multiple suppliers. This paper presents a specification overview, as well as an application-specific example identifying the strategic benefits of the specification for embedded system development.

**Mercury Computer Systems, Inc.**

<http://www.techbriefs.com/wp/8366>



## New! Software Defined Radio Handbook, 8th Edition

The folks at Pentek, who wrote the book on software radio, are pleased to announce their recently released and expanded 2010 Software Radio Handbook. Now in its 8th edition, the handbook shows how DDCs and DUCs, the fundamental building blocks of SDR, can replace conventional analog receiver designs, offering significant benefits in performance, density and cost. As such, it is a useful technical reference for engineers. It's yours free, just click on the link below to download a copy.

**Pentek, Inc.**

<http://www.techbriefs.com/wp/8348>



## Simplifying Embedded FPGA Development with BittWare's ATLANTIS FrameWork Methodology

While FPGAs provide significant performance benefits, the FPGA development process can be both time-consuming and difficult. BittWare's ATLANTIS FrameWork (AFW) addresses these limitations by providing infrastructure that supports FPGA development at a higher abstraction level, enabling AFW customers to move quickly and confidently from design to deployment.

**BittWare, Inc.**

<http://www.techbriefs.com/wp/8367>

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