

VITA Standards Organization Update

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VITA was accredited as a Standards Development Organization (SDO) in June 1993 using the ANSI Canvass Ballot method and holds standards meetings every two months to work on standards issues of interest to its members.

Currently the VITA Standards Organization (VSO) is working on a variety of standards that include extensions to the VME64 specification, P2 buses standards, software standards, and various form factor standards.

If you are working on a technology that fits within the scope of the VSO and feel that the standardization of that technology would be of benefit, please contact John Rynearson, Technical Director for

more information about the VITA Standards Organization.

The next two VSO meetings are scheduled for May 1998 in Phoenix and July in Santa Fe NM.. Surf VITA's web site at <http://www.vita.com/vso/std.html> for agenda, registration, and previous meeting minutes information. Many draft specifications are available in PDF format and may be downloaded free of charge from VITA's web site.

RECOGNIZED STANDARDS

The following standards have been recognized as American National Standards by successfully completing the ANSI canvass ballot process. Anyone who is materially or directly affected by a standard may participate in a canvass ballot

or alternately they may provide comments to VITA via the ANSI public review process. Participants do not need to be members of VITA to ballot VSO sponsored standards during the ANSI ballot process.

ANSI/VITA 1-1994, VME64- The VME64 Specification brings a number of new features to the VMEbus, such as 64 bit data transfers for 6U modules, 32 bit data transfers for 3U modules, rescinding DTACK, lock commands, RETRY signal, auto slot identification, auto system controller enable, and configuration ROM (CR) and control/status registers (CSR). This specification was officially recognized as an American National Standard

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The 68000 (I>M, I>A) and 68060 (I>M, I>A) CPU cards show two positive market conditions out of the three possible combinations implying growth in those segments. The reason for the 68000 CPU cards positive market factor, however, is related to declining product availability due to many manufacturers withdrawing old 68K product offerings. The 68060 positive market conditions are probably due to upgrade potential from the 68040 CPU cards since there's software compatibility in the 68K family. The 88K shows negative market factors, which is not surprising. The PowerPC shows the greatest positive market factors (M>A, I>A) which implies growth in this segment.

The Intel family of CPUs on VME show 80486 (A>M, A>I) and i860/960 (A>M, A>I) with two negative market factors. The 80386 cards are slightly positive due to legacy software and limited product availability. But, the 586 (I>M, I>A), the Pentium (I>M, I>A), and the Pentium Pro (I>M, I>A) all show high positive market factors. Interest in the market is high for each of these processor types on VME CPU cards.

The SPARC CPU card segment (I>A, M>A) show positive market growth factors but only because it's a niche market segment. The MIPS architecture (I>M, I>A) is positive for the same reasons and

the limited availability of products. The HP-PA segment (I>A, M>A) shows growth potential for the same reasons as the Alpha processor (I>M, I>A) on VME. And, the 29K series of CPU cards (I>M, I>A) show growth potential due to low product availability and low market share compared to the interest levels, but this is probably because of legacy software issues similar to the 88K.

When we remove the niche CPU segments and all the legacy interest of older CPU types, the highest market growth potential in VME CPU cards boils down to the Pentium (+10) and the PowerPC (+6) CPU types. While the 68040 shows negative market factors, this is just a reflection that this segment is saturated with products and the market share is peaking. Many new design-ins are occurring with the 68040, but they are being won by established companies in the market. The negative market factors in the table show the resistance to new 68040 or 68030 cards entering the market, not overall market growth.

While this statistical analysis didn't tell us anything particularly new, it did put numbers on our assumptions and market observations. Looking at the interest levels from the pings on the VITA web pages would be misleading if we didn't compare that to both the market share and the availability of products.

From the chart, you can see that the PowerPC has the highest overall interest level (15% of the pings), followed by the Pentium (9% of the pings). The market is moving toward the PowerPC for hard real-time applications, while the Pentium pings show the interest in soft real-time applications and the Microsoft software environment. In general terms, the VME CPU market seems to be splitting into those two primary segments while the SPARC, HP-PA, and Alpha CPUs show high interest from the embedded UNIX applications segment. And, the 68K market segment is most influenced by legacy issues and upgrade potential for its growth in the future.

Overall, there were 12 positive growth segments in the VME CPU market, and 7 negative-growth CPU segments, still a healthy environment for most manufacturers. But, there is product and market-share saturation in some of those segments. As new CPU types come to the VMEbus on new CPU card introductions, this picture will change during 1998. We will track these statistics during the year and continue this analysis in the future here at VITA. The CPU board segment of the VME market is almost \$800 Million, or 63% of the \$1.25 Billion total VME board market. So, it's important to learn as much as possible about how this market segment behaves, and to gain some insight into its trends.

on April 10, 1995 and is available from the VITA office.

ANSI/VITA 3-1994, Board-Level Live Insertion for VMEbus- The Board-Level Live Insertion (BLLI) specification is a recommended practices document for live insertion of VMEbus modules. This document identifies a standardized methodology through which a faulty board can be removed from a system and a replacement board can be inserted while the system continues to operate. The intent of this standard is to provide a methodology that will work with currently existing boards. This specification was officially recognized as an American National Standard on January 12, 1996 and is available from the VITA office.

ANSI/VITA 4-1995, IP Modules- Mezzanine modules add functionality to base level circuit boards. On VME, IP Modules can be used to create a custom VMEbus board by selecting the functions needed for a specific application. IP Modules are approximately the size of a business card. Four modules can be placed on a single VMEbus module. This specification was officially recognized as an American National Standard on July 16, 1996 and is available from the VITA office.

ANSI/VITA 4.1-1996, IP I/O Mapping to VME64x- This draft standard creates a standard I/O pin assignment map between IP Modules (ANSI/VITA 4-1996) and backplane I/O pins as specified in draft standard VITA 1.1-1997, VME64x. This specification was officially recognized as an American National Standard on March 3, 1998 and is available from the VITA office.

ANSI/VITA 5-1994, RACEway Interlink- RACEway Interlink is a standard for a parallel-based cross-bar switched interconnect on the P2 connector of the VMEbus. Data rates for a single RACEway interconnect are 160 Mbytes/sec peak and 150 Mbytes/sec sustained. This specification was officially recognized as an American National Standard on July 31, 1995 and is available from the VITA office.

ANSI/VITA 6-1994, Signal Computing System Architecture (SCSA)- SCSA stands for Signal Computing System Architecture and is used for processing digitized voice, video, and digital data in

telephony applications. This specification was officially recognized as an American National Standard on July 24, 1995 and is available from the VITA office.

ANSI/VITA 6.1-1996, SCSA Extensions- The purpose of this draft standard is to define the J2/P2 pin assignment and operating modes of additional SCbus bearer channel (time slot) capacity and to define a redundant set of SCbus controls. This document provides several nested levels of capacity with increasing redundancy features, each of which is oriented towards specific segments of the computer telephony market. This specification was officially recognized as an American National Standard on February 20, 1998 and is available from the VITA office.

ANSI/VITA 10-1995, SKYchannel Packet Bus on VME P2- SKYchannel is a high performance 320 Mbyte/sec packet switched architecture. This specification was officially recognized as an American National Standard on October 31, 1997 and is available from the VITA office.

ANSI/VITA 12-1996, M-Modules- M-Modules are small printed circuit boards that can be used to add functionality to a base level motherboard through a standardized interface. This specification was sponsored by the VITA members of MUMM, the Manufacturers and Users of M-Modules and was officially recognized as an American National Standard on May 20, 1997. ANSI/VITA 12 is available from the VITA office.

ANSI/VITA 13-1995, VMEbus Pin Assignment Standard for IEC 14475 (IEEE Std 1355-1995) Heterogeneous Interconnect (H.I.C.) on VME- HIC (Heterogeneous InterConnect) is a serial bi-directional, high-speed data transfer interface between processor boards, subsystems, or multiple computer chassis. This specification was officially recognized as an American National Standard on July 16, 1996 and is available from the VITA office.

DRAFT STANDARDS IN THE ANSI CANVASS PROCESS

The following standards have met the 75/75 criteria within the VSO. That is, they have received 75% approval of 75% of the returned ballots of a formal VSO task group ballot. Standards which meet this criteria move to the ANSI canvass ballot process.

VITA 1.1-1997, VME64x, (Extensions to VME64)- During the development of the VME64 specification a number of proposals were discussed. In order to complete the VME64 specification in a timely manner, certain proposals were put into the category of VME64 extensions to allow more time for investigation and discussion. Wayne Fischer, Force Computers is chair of the VME64 extensions task group. At the September 1997 VSO meeting VITA 1.1 was moved to ANSI canvass ballot. VITA 1.1 is currently under ballot in the ANSI canvass ballot process. The ballot period ends March 27, 1998.

VITA 1.3-1997, 9U x 400 mm VMEbus Form Factor- The purpose of this group is to standardize a 9U form factor for use in VME. A draft document is available from the VITA office. This draft standard has been moved to ANSI canvass ballot. Bob Downing, Fermi, rwd@fnal.gov, is the task group chair of this activity. VITA 1.3 is currently under ballot in the ANSI canvass ballot process. The ballot period ends March 27, 1998.

VITA 14-1997, CXC and ModPacks, Draft 2.5, January 12, 1996- CXC is based on the 68302 controller bus and ModPacks are used to add functionality to the CXC base module. This document will be used to standardize an existing industry practice originally developed by PEP Modular Computers. An initial task group ballot was completed in April and this standard will be submitted to the ANSI canvass process. Currently the ANSI ballot list is being constructed.

VITA 19-1997, BusNet- BusNet enables multiple CPU boards (and/or intelligent controller boards) to communicate across a backplane as if it were an Ethernet network. BusNet permits system configurations consisting of UNIX, real-time or mixed UNIX/real-time computing nodes to exist within one single chassis. A copy of the Busnet draft standard is available from the VITA office. A task group ballot for Busnet was completed on May 23, 1997 and VITA 19 has been moved to the ANSI canvass process. Contact John Rynearson, Technical Director, VITA (techdir@vita.com) if you wish to ballot this standard. A copy of the Busnet specification is available on VITA's web site.

VITA 23-1997, VMEbus for Physics Applications- Many particle physics labs use VME as the basis for experiment control. The purpose of this effort is to come up with a set of recommended practices to encourage commonality. This effort is being sponsored by VIPA — the VME International Physics Association. Contact Bob Downing, Fermi, rwd@fnal.gov, or Chris Parkman, CERN, chris_parkman@cern.ch, for more information regarding this effort. The last task group ballot met the VSO's 75/75 rule and VITA 23 has been moved to the ANSI process. If you would like to participate in the ANSI ballot of this standard, please contact John Rynearson <techdir@vita.com> or Cheryl Cook <cheryl@vita.com> at VITA.

VITA 25-1997, VISION- At the July 1996 meeting in Ottawa, Jim Pangburn of Fermi National Accelerator Laboratories presented a proposal for an object based I/O software interface for the VMEbus. To build consensus for this effort Jim asked and was granted study group status. At the September 1996 VSO meeting, task group status was granted when CERN, Lecroy, and Fermi indicated that they would sponsor this effort. A draft specification is available on the VITA web site. The group has completed a successful task group ballot and VITA 25 has been moved to the ANSI canvass process. Contact John Rynearson, VITA, <techdir@vita.com> or Cheryl Cook, VITA, <cheryl@vita.com> if you want to participate in the ANSI ballot.

VSO TASK GROUP ACTIVITIES

Standards within the VSO are developed in task groups. The formation of a task group requires at least three companies that are VITA members and the proposed work must fit within the defined scope of VITA's accreditation with ANSI. Non VITA members may serve on task groups with the approval of the chair and the task group. The following draft specifications are being developed by their respective task groups within the VSO.

VITA 1.2-199x, High Availability VME (H. A. VME), Draft 0.2, Nov. 9, 1995- This work is a result of the work started as VMEbus System Level Live Insertion. At the Orlando VSO meeting in March 1995 a special meeting was held to discuss High Availability VMEbus (H.A. VME) requirements. The purpose of this group is to develop a standard based on VME64 and VME64 Extensions that provides

Scaleable Fault Management and Dynamic Configuration in Live Systems. Issues to be addressed include: fault detection, fault isolation, fault repair, and live insertion. It was realized that not all applications require all the features and that scalability is an important issue. During the November 1996 VSO meeting, Lou Francz, Dialogic, proposed that a separate standard addressing live insertion be developed using much of the work already done for H.A.VME. He argued that this standard could be completed in a short period of time and would address current market needs. The membership agreed and a task group to develop a live insertion specification (see VITA 1.4) for VME64x was formed.

VITA 1.4-199x, Live Insertion for VME64x- This effort is an outgrowth of the VITA 1.2, High Availability task group. Lou Francz is task group chair and a draft specification for VITA 1.4 is available from the VITA office. Contact Lou Francz at franczl@dialogic.com for more information on this specification.

VITA 1.5-199x, Source Synchronous Transfer Protocol- At the 1997 Real Time Computer show in Santa Clara, California, Drew Berding of Arizona Digital demonstrated a new VMEbus backplane that allows data to be transferred at rates of 320 Mbytes/second. To take advantage of this new technology, the VSO set up a task group to develop a source synchronous protocol. The task group has completed much of its work and the draft specification is available on VITA's web site.

VITA 1.6- 199x, Keying for Conduction Cooled VME- This task group is developing a method to provide slot specific keying for conduction cooled VMEbus modules. Holly Sherfinski, HARTING, INC., is task group chair. The first task group ballot was completed successfully and negative ballots were reviewed and resolved at the January 1998 VSO meeting. The draft standard will be recirculated and then submitted to the ANSI process. Contact Holly at <holly.sherfinski@harding.com> regarding this draft standard.

VITA 5.1-199x, Extensions to RACEway Interlink- The purpose of this task group is to extend RACEway Interlink to take advantage of the new 160 pin connector. The task group chair is Tony Lavelly, Mercury Computer. Contact Tony at atl@mc.com.

VITA 11-199x, Autobahn- Autobahn technology promises high speed bused and point to point data links with data rates of 200 Mbytes/sec. Current Autobahn chips have demonstrated data rates of 50 and 100 Mbyte/sec. The Autobahn draft specification is available from the VITA office. Contact Hermann Strass, Technology Consulting, +49 89 601 34 99, fax: +49 89 601 23 29, email: TechCon.HStrass@t-online.de for more information about this effort.

VITA 17-1998, FPDP- FPDP stands for Front Panel Data Port and is a proposed standard being put forth by Interactive Circuits and Systems, Ltd. with support provided by SKY Computers, Ixthos, and CSPI. Task group status was granted at the January 1995 VSO meeting. FPDP is an existing industry practice specification developed to provide high speed data transfer using front panel data ports. Data transfer rates of 80 Mbytes/sec are possible using the FPDP interface and 160 Mbytes/sec are possible using the FPDP2 interface. The draft was recently updated and a successful task group ballot was held. FPDP will be moved to the ANSI canvass ballot process shortly. Contact Jonathan Jones, ICS, (613) 749-9241 if you are interested in FPDP.

VITA 18-1998, VMEbus on SEM-E- SEM-E has been a popular form factor used in the military for a number of years. It is based on conduction cooled technology, a small form factor, and a blade & fork style connector that provides high reliability in high shock and vibration environments. A draft of this document is available from the VITA office. Currently optimal pin assignments are under investigation. A successful task group ballot was completed and the results were presented at the January 1998 VSO meeting. VITA 18 will now be submitted to the ANSI process. Contact the VITA office if you are interested in balloting this standard.

VITA 20-199x, Conduction Cooled PCI Mezzanine Card- The purpose of this effort is to develop a standard for a conduction cooled PMC card based on IEEE 1386 and IEEE 1386.1 for conduction cooled VMEbus boards. This group was granted task group status at the January 1996 VSO meeting. A draft of VITA 20 is available from VITA's web site. Contact Doug Patterson, DY4, dpatterson@dy4.com for more information about this effort.

VITA 22-199x, Cells Bus on VME- Cells Bus is an ATM multiplexing and switching technology that could be used on the P0/J0 connector to provide ATM access across the VMEbus backplane. TranSwitch is supporting the development of this draft standard. A copy of VITA 22 is available from the VITA office.

VITA 26-1998, Myrinet- At the January 1997 meeting in Santa Clara, a new activity called Myrinet was proposed to the VSO. Myrinet is a high-speed (gigabit-per-second) packet communication and packet-routing technology that is used both as a system-area-network (SAN) and a local-area-network (LAN). Three VITA members, CSPI, AMP, and Myricom have agreed to support the standardization of Myrinet. The results of the task group ballot were presented at the January 1998 VSO meeting. All negative ballots were resolved and VITA 26 will be submitted to the ANSI canvass ballot process. If you are interested in balloting this standard or providing comments, please contact the VITA office.

VITA 27-199x, P2CI- At the July 1997 VSO meeting in Vancouver, BC, a new activity called P2CI was introduced by Robert Negre, CETIA. The purpose of this effort is the mapping of the PCI bus onto the P2 VMEbus user defined pins. Task group status was granted in August and the group is developing the draft standard. A rough draft with proposed pin assignments is available on the CETIA web site in PDF format at: <http://www.cetia.com/product/technology/p2cispecV0.2.pdf>.

Contact Serge Tissot, CETIA, <st@cetia.fr>, for more information about this effort.

VITA 28-199x, VPCI- At the July 1997 meeting in Vancouver, BC, Rick O'Connor, Tundra, discussed the feasibility of creating a virtual PCI bus across the VMEbus backplane. This concept would allow a VME module with a PCI local bus to communicate directly with another VME module with a PCI local bus using standard PCI based bridge software.

Contact Jonathan Morris, Tundra, jonm@tundra.com, if you are interested in this effort.

VITA 29-199x, PC•MIP- PC•MIP is a mezzanine concept being promoted by MEN Mikro Elektronik and Greenspring. MEN, SBS GreenSpring, and Motorola Computer Group have agreed to sponsor a VITA Task Group to work towards international standardization. Contact the VITA office for more information on the PC•MIP standardization effort.

VSO STUDY GROUPS

TEMPE- Jim Botte, NORTEL, introduced a concept called TEMPE, Telecommunications and Enterprise Multimedia Platform and Environment. TEMPE is an amalgamation of standard technology, extensions to that technology, and proprietary technology licensed from multiple companies integrated, and presented as a new open standard. Contact Jim Botte, NORTEL, jbotte@nortel.ca