

Radar DSP System Uses Multi-SHARC I/O Processor Board

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The Analog Devices 40 MHz AD21062 SHARC is a 32-bit floating-point DSP processor optimized for demanding signal processing applications. Fabricated in a high-speed CMOS process, it has a 25-nsec instruction cycle time and operates at 40 MIPS. With its on-chip instruction cache, the processor can execute every instruction in a single cycle.

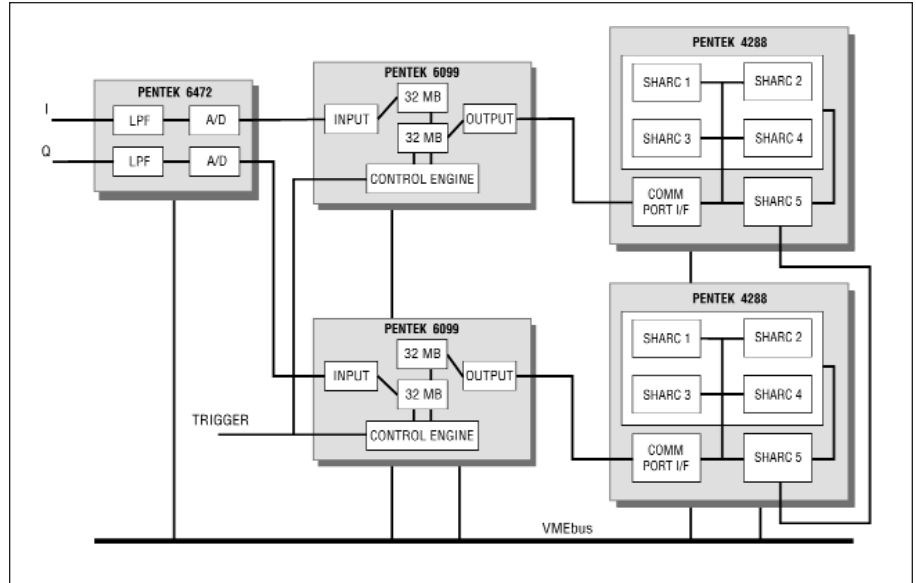
The SHARC performs a 1024-point complex FFT in 460 msec. This benchmark represents a new standard of performance for DSP processors and was of prime importance in implementing a radar DSP system with standard off-the-shelf VME boards from Pentek by one of its customers.

System Requirements

Some of the system specifications include capturing 1024 samples of the radar pulse which occurs every 150 msec, processing in-phase and quadrature (I and Q) complex data at a sampling rate of 70 MHz and performing a 1024-point complex FFT on the data.

The heart of the system is the new Pentek 4288 Multi-SHARC I/O Processor VME board. It provides scalable architecture and connectivity with a wealth of I/O peripherals available from Pentek. Its many interface options include, among others, SHARC link ports, comm ports, VME64 master/slave interface, Ethernet and RS-232. A SHARCPAC mezzanine expansion site allows for increasing the number of processors on the board from one to seven. Memory resources include generous amounts of SRAM, SDRAM and flash memory. An optional PowerQUICC controller, a highly integrated power PC, manages data flow, VME resources and interfaces.

The Pentek 6472 two-channel A/D Converter was selected to digitize the data. Capable of sampling to 70 MHz with 10-bit accuracy, it met system specifica-



Radar DSP System uses Pentek VME boards including two Model 4288 Multi-SHARC I/O Processors.

tions. In addition, two Pentek 6099 Dual Buffer Memory boards which accept up to 16-bit samples at a 70 MB/sec rate were included to capture the I and Q radar pulse data and unload each of their two buffer memories into the SHARC processors for FFT computations. The two buffers of the 6099 are arranged in a "swinging buffer" configuration; while one buffer is filling, the second one is emptying the data.

System requirements dictate that the FFT calculation be performed during the length of the radar pulse, or every 150 msec. Since the SHARC FFT calculation takes 460 msec, it becomes necessary to use four SHARCs in parallel processing to achieve real-time performance. A fifth SHARC is also utilized for data distribution via the link ports to the four SHARCs. The Pentek 4288 Multi-SHARC Processor board was therefore outfitted with five processors to meet system specifications and two such boards are used to process

the I and Q data streams. The two outputs are then combined into a complex result via the link port connection of the fifth SHARC.

Signal Connections

The analog input signals are connected to the two channels of the A/D converter through convenient front panel SMA connectors. The digitized outputs are then brought out to parallel digital front panel connectors which are connected to identical front panel input connectors of the buffer memory board with flat cables. The outputs of the buffer memory boards are then connected to the processor board via the boards' front panel comm ports. The FFT data are delivered over the VMEbus for display, storage and off-line post-processing.

Pentek is on the web at: <http://www.pentek.com>