

Selecting a PowerPC for Embedded Applications

Courtesy of SKY Computers

The PowerPC 604e microprocessor has always been the high-end performer in the PowerPC product line. Specifically optimized for scientific applications and targeted for high-end desktop, workstation, and multiprocessing systems, the 604e microprocessor has many features not found in any other PowerPC microprocessor. With the recent introduction of the low power version of the PowerPC 750 microprocessor, choosing the best processor to fit the application can be confusing. For the embedded market, two of the most important unique features of the 604e are the ability to pipeline memory accesses and the inclusion of a third integer execution unit. These result in higher sustained memory bandwidth and lower overhead for DSP functions.

Simple vector functions like a single precision real vector multiply run 1.6 - 1.8 times faster on a 604e than on a 740 or 750 microprocessor when the data goes to and from memory. When the data is preloaded in cache, the 604e is still 1.5 times faster than a 740 or 750. For more computationally intensive functions such as FIRs and FFTs, the speed-up is approximately 33% faster. For example, a 1024 real FIR filter with 32 taps runs 30% faster on a 604e than on the 740 or 750. A 1024 point complex FFT runs 43% faster on a 604e than on either the 740 or the 750. There are many other features that impact real time embedded applications, including those summarized in Table 1.

604e Microprocessor Upgraded to .25 Micron Process- Initially the PowerPC 604e microprocessor had a power consumption of 18W, which effectively prohibited its use in multiprocessor VME applications. At that time, the only PowerPC choice for floating-point intensive embedded system applications was the PowerPC 603e. Next the PowerPC 740 and 750 microprocessors were introduced, which share a common die and were optimized for Macintosh applications. The availability of the 740/750 microprocessors provided larger caches and a second integer unit, which prevent-

ed the floating-point pipeline from stalling as often. While there were still some floating point stalls, the biggest remaining problem was the sustained memory bandwidth. The theoretical best sustained memory bandwidth from either a 603e microprocessor or a 740/750 microprocessor is about 40% of the peak, with 30% representing a more typical achievement.

IBM and Motorola surprised the world by taking the 604e microprocessor to a new .25 micron process that resulted in a 33% speed up in the processor clock and a 300% reduction in power consumption. The new 604e microprocessor, sometimes called the 604r or "Mach5", makes the top-of-the-line performance available to the embedded multiprocessor industry.

604e Microprocessor: Highest Sustained Memory Bandwidth- For memory bandwidth limited applications, such as most digital signal processing, the performance of the external processor interface is just as important as CPU speed. If the memory bus cannot feed the processor, the fast CPU spends its cycles just spinning idly.

For the most part, an L2 cache does not help much for DSP applications, because either the data typically is small enough to fit into the on-chip cache or is not reused sufficiently to receive much benefit for the extra cost, power, and board space of an L2 cache.

The PowerPC 604e microprocessor has 64-bit external interfaces that can operate at 83.3 MHz, yielding a 667 MB/sec peak memory bandwidth. The new version of the 750 increases the external interface frequency to 100 MHz, yielding a peak bandwidth of 800 MB/sec. However, the 604e still provides higher sustained memory due to its capability to pipeline data memory accesses.

When a new vector of data needs to be read, burst reads are employed by the microprocessor. A single address in the request results in four consecutive memory datawords returned. Thus the latency for the first access is avoided for the subsequent accesses in the burst. If the vector is longer than four words, another burst read is requested and another latency occurs before the burst is returned. If the second burst can not be requested until the first burst is complete, the gap

	603e	740	750	604e
Maximum Processor Clock	300 MHz	300 MHz	400 MHz	333 MHz
Maximum Bus Clock	75 MHz	83.3 MHz	100 MHz	83.3 MHz
Peak Memory Bandwidth at Maximum Clock	600 MB/sec	667 MB/sec	800 MB/sec	667 MB/sec
Sustained Memory Bandwidth at Maximum Clock (typical)	160 MB/sec	200 MB/sec	240 MB/sec	440 MB/sec
Memory Streaming	no	no	no	yes
Sustained Memory Bandwidth at Maximum Clock (With Prefetch)	400 MB/sec	445 MB/sec	553 MB/sec	667 MB/sec
Cache Size (I/O)	16K/16K	32K/32K	32K/32K	32K/32K
Floating Point Multiplier	32-bit	32-bit	32-bit	64-bit
Integer Units	1	2	2	3
Completion Rate	1 instruction	2 instructions	2 instructions	4 instructions + 1 store and 1 branch
Branch Prediction	static	dynamic	dynamic	

Table 1.

between the first burst and the second burst is the full latency of the memory system plus a cycle or two for the request to be issued and the data to be latched.

Memory pipelining drastically reduces that latency allowing the second burst read to be issued before the first one is requested. This overlaps the access latencies for the two accesses and significantly reduces the gap between the data bursts.

The PowerPC 604e microprocessor supports memory pipelining for burst data reads, while the 750 microprocessors does not. The result is that the 604e microprocessor has almost double the sustained memory bandwidth of the 750 microprocessor.

604e Microprocessor: More Integer Units to Handle DSP Overhead - When applying any general purpose microprocessor to signal processing applica-

tions, the effects of DSP overhead are a concern. Microprocessors specifically designed for DSP often have specialized hardware to take care of this overhead. For example, separate loop counters provide zero-overhead-loops and direct address generators free the main execution unit from stopping execution of the arithmetic operations in order to calculate addresses.

General purpose microprocessors accomplish these same tasks with extra execution units. The PowerPC 740/750 microprocessor adds a second fixed-point unit to that of the 603e microprocessor design. The number of execution units is six, including two fixed-point units, a floating-point unit, a branch unit, a load/store unit, and a system unit. However, these processors are capable of completing only two instructions plus a branch every cycle, thereby limiting the

extent of the superscalar performance and frequently stalling the floating point pipeline.

The PowerPC 604e microprocessor is capable of completing four arithmetic instructions plus a branch and a store each cycle, thus the 604e microprocessor is able to more fully utilize its superscalar architecture. An extra help for DSP applications is a third integer unit, bringing the total number of execution units to seven. These extra integer units are very useful for address calculations and other overhead functions which dramatically reduces floating point stalls. The 604e microprocessor is architected to achieve a higher sustained performance on scientific and signal processing applications than any other PowerPC microprocessor architecture available today.

SKY Computers is on the web at: www.sky.com

New Products Gallery

CETIA, Inc. has announced a new family of PowerPC SBCs—the PowerEngine 5 family—targeted at embedded and military applications. Available in either mono or dual processor configurations for performance and design flexibility, each processor has a dedicated 1MB of backside L2 cache, allowing both PowerPC 750 microprocessors to run in parallel. The use of a separate L2 cache bus enables up to a three times processing increase than earlier cache designs. CETIA is on the web at www.cetia.com

Concurrent Technologies has announced its first Pentium II based single-slot PC compatible VME board; the VP PSE/P22. Based on the latest Intel Pentium II Mobile Module the board addresses the rapidly growing demand for high performance Intel CPU architectures in the VME market while satisfying the market's need for low power consumption, low physical profile, high-performance, high reliability and extended product life. The VP PSE/P22 uses the latest 0.25-micron technology Pentium II Mobile Module. Today's Mobile Module provides a Pentium II

processor operating at 266MHz with 32 Kbytes of L1 cache and 512 Kbytes of L2 cache and utilizes the high-performance 440BX chipset. Concurrent Technologies is on the web at: <http://www.cct.uk> as well as <http://www.gocot.com>

American ELTEC has introduced the Basic Automation Board (BAB) 740, which is a VMEbus CPU board containing a PowerPC processor and PMC extension capability that has been optimized for use in industrial automation and image processing applications. The available PMC modules consist of a graphics controller with two independent graphics controllers on the same module and a frame grabber with full DMA into processor memory. American ELTEC is on the web at: www.eltec.com

MATRIX Corporation has announced the GMO Rugged Enclosure, another in the series of All-Terrain Enclosures. The GMO is an off-the-shelf solution optimized for use in ground mobile/vehicular, portable system, and other high shock and vibration applications. The enclosure's features include

superior airflow, unique EMI shielding techniques, and an improved cushioning design. Flowthrough air cooling provides over 200 cubic feet of air per minute. To reduce EMI radiation, the GMO has conductive interior surfaces, conductive gaskets, and honeycomb shielded vent screens covering all openings. The enclosure is made of aluminum for light weight. A skin-on-frame design creates a very rigid exterior shell. MATRIX is on the web at: www.matrix.com

2 new PC•MIP mezzanine cards have been announced by **MEN Mikro Elektronik**. The P3 is a standard Ethernet interface based on the Ethernet controller DS21041 by DEC. It supports 10BaseT via a 9-pin D-Sub connector at the front panel. The P3 has a high 2kV isolation voltage and offers full duplex support. The PC•MIP is ready to run with the standard Plug and Play driver for Windows95/WindowsNT by DEC. The model P4 is a fast SCSI interface based on the SCSI controller SYM53C895 by Symbios. It supports Ultra2 SCSI up to 40MB/s in single-ended (Fast SCSI and Ultra SCSI modes),

and LVD (Ultra2 SCSI mode) signaling environments as well as big/little endian. MEN is on the web at: www.men.de

Motorola Computer Group has announced the PowerPlus II VME Architecture as well as the first product based on it, the MVME2400 single board computer. The PowerPlus II VME Architecture features a new integrated chip combining a 64-bit PCI host bridge and 144-bit ECC memory controller. Features in the PowerPlus II VME Architecture include support for 100 MHz local bus operation and utilization of synchronous DRAM (SDRAM) technology. The MVME2400 combines the PowerPlus II Architecture with a 233 or 350 MHz PowerPC 750 microprocessor, optional 1MB of backside Level 2 cache and dual PMC slots to deliver outstanding performance in a single VME slot.

PowerPlus II VME Architecture enhances the estimated peak SDRAM bandwidth to 582 MB per second and further reduces bandwidth bottlenecks for real-time embedded computing. By integrating functions previously

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