

VITA 2.1-199x Task Group

The development of a standard defining new ETL-like ICs for supporting 2eVME & 2eSST protocols at maximum design speeds

VITA 2.1-199x Task Group - Basic Goal

- **Goal: New commercial ICs which allow 2eVME & 2eSST operations at maximum design speeds:**
 - ◆ In new VME64x and/or legacy backplane subracks
 - ◆ Under all module bus loading conditions
 - ◆ With any mixture of old legacy modules and modules using the new ICs
- Simulations should be used to determine if all or just parts of the goal are possible
- Can the primary goal be achieved?
- Some of the following restrictions **may** be necessary:
 - ◆ 2eSST and/or 2eVME modules with 5-row connectors
 - ◆ Backplanes with 5-row connectors
 - ◆ No 3-row legacy modules!
 - ◆ All data lines loaded equally!
 - ◆ Etc.

VITA 2.1-199x Task Group - Course Of Action

- Hopefully obtain support from IC vendor(s)
 - ◆ TI & Fairchild
- Add new task group members
- Define simulation goals & list of initial simulations
- Request LLC and/or additional VSO funds for helping company which does simulations
- Write initial standard

VITA 2.1-199x Task Group Organization

- **Three Initial Supporting VSO Members:**
 - ◆ TreNew
 - ◆ Motorola
 - ◆ Fermilab
- **Task Group Members To Date:**
 - ◆ Andreas Lenkisch
 - ◆ Mac Rush, Motorola
 - ◆ Bob Sullivan, Hybricon
 - ◆ Mike Thompson, Schroff
 - ◆ Wayne Fischer (retired)
 - ◆ Ron Seese, Chrislin Industries
 - ◆ Eike Waltz, Rittal
 - ◆ Bob Downing, Fermilab (consultant)
 - ◆ Ed Barsotti, Fermilab
- **Sign up sheet being passed around at this time**

VITA 2.1-199x Task Group - Initial Basic Features For The New ICs

- VITA 2-199x ETL-like receiver characteristics for receivers which would connect to the VME bus. Due to tight 2eSST source, bus & receiver skew specifications, present ETL receiver input thresholds may need to be changed
- Controlled rise and fall time drivers (four to five nanoseconds?)
- Normal VME64 bus driver current capabilities or 'softer' drive???(needs to be reviewed ... & backwards compatible)
- Bias pin & circuitry for live insertion?
- Guaranteed and minimal input to output skew, pin to pin & IC to IC
- Low simultaneous output switching noise
- Clocked or transparent input registers for:
 - ◆ Controlled input to output skew of drivers
 - ◆ Optionally latching input bus signals
- Surface mount & other packaged devices
- Possibly pin compatible to VITA 2 - 199x specifications

VITA 2.1-199x Task Group - Is ETL The Right Choice For The New ICs? (prompted by comments from Mac Rush)

- ETL parts have low volume therefore it is difficult to get IC vendors interested
- Are all ETL features necessary?
- What about modifications to the high-volume, multiple-sources LVT parts?
- Some LVT features:
 - ◆ Powering up in the 3-state mode for live insertion applications
 - ◆ Internal device output series damping resistors
 - ◆ Symmetrical high to low & low to high output drive currents
 - ◆ + 3.3 volt operation
- ETL, LVT & GTL - We need to look at all three technologies
 - ◆ ETL - Enhanced Transceiver Logic
 - ◆ LVT - Low Voltage BiCMOS Technology
 - ◆ GTL - Gunning Transceiver Logic

VITA 2.1-199x Task Group - Initial List of Needed Simulations

- Initial attempt to list the different combinations of parameters needing to be simulated in order to properly specify VITA 2.1-199x transceivers:
 - ◆ Output driver input clock to output stable skew times pin to pin and IC to IC
 - ◆ Output drive characteristics with various controlled rise and fall times
 - ◆ Receiver input threshold sensitivity differences (minimum high-level input voltage to maximum low-level input voltage differential) and various absolute receiver input switching levels
 - ◆ Receiver input clock to output stable skew times pin to pin & IC to IC

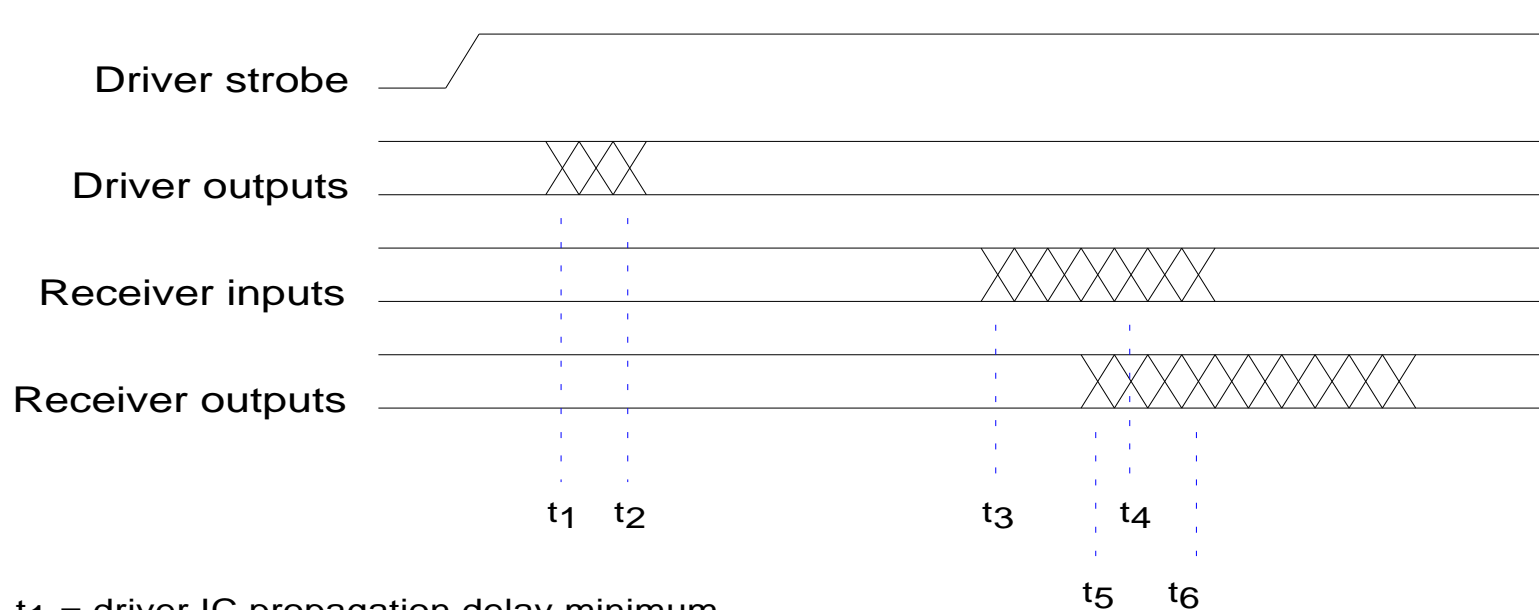
VITA 2.1-199x Task Group - Initial List of Needed Simulations (continued)

- ◆ In legacy and VME64x backplanes, various bus loading conditions including various combinations of legacy and VITA 2.1-199x compatible modules and including the effects of different amounts of drivers and/or receivers on certain data and other signal lines (e.g., D08 modules mixed with D32 modules)
- ◆ Acceptable simultaneous driver output switching noise for all the above variations
- **Some reasonable subset** of all the simulation possibilities given above will have to be decided upon so that a practical amount of simulations can be done to determine required device characteristics.
- A draft list of needed simulations for review will be completed within a few weeks
- It appears that simulations such as these are also needed to properly complete the 2eSST specification

VITA 2.1-199x Task Group - Additional Simulations Comments & Questions

- Controlled and slower than usual rise and fall times might dictate smaller receiver input threshold sensitivity (minimum high-level input voltage to maximum low-level input voltage differential) specifications to insure reliable reception of data when 2eVME and especially 2eSST operations are occurring at the highest design speeds.
- Is it possible to only require the longer controlled rise and fall times during the worst loading conditions and still have 2eVME and 2eSST protocols work over 21 slots with any mixture of VITA 2.1-199x compatible and non-compatible ETL receivers on the bus and any distribution of bus loading?
- What is the range of controlled rise and fall times that can be maintained over the range of loading and receiver input threshold sensitivity?

VITA 2.1-199x Task Group - Some Timing Considerations



t_1 = driver IC propagation delay minimum

t_2 = driver IC propagation delay maximum

$t_2 - t_1$ = input to output skew (propagation delay) difference pin to pin & IC to IC

t_3 = bus loading propagation delay minimum

t_4 = bus loading propagation delay maximum

$t_4 - t_3$ = bus loading skew (propagation delay) difference for any loading & for any backplane

t_5 = minimum receiver threshold logic 0/1 detection time + minimum receiver IC input to output skew pin to pin & IC to IC

t_6 = maximum receiver threshold logic 0/1 detection time + maximum receiver IC input to output skew pin to pin & IC to IC

$t_6 - t_5$ = receiver IC threshold logic 0/1 detection time difference + receiver IC input to output skew (propagation delay) difference pin to pin & IC to IC

VITA 2.1-199x Task Group - VSO Companies Expressing Interest In Doing Simulations

- VSO companies which have expressed an interest in doing simulations:
 - ◆ TreNew - Andreas Lenkisch
 - ◆ Hybricon - Bob Sullivan

VITA 2.1-199x Task Group - Initial IC Company Contacts

- Texas Instruments - Shankar Balasabermaniam, Adam Ley and Ramzi Ammar
 - ◆ Initially very interested
 - ◆ Low-voltage ETL
 - ◆ March conference call results
 - ✦ Had started planning on new backplane transceivers
 - ✦ LVTE possibly
 - ✦ We need to know our requirements - simulations, simulations
 - ✦ They will also do simulations
 - ✦ No commitment to date
- Fairchild Semiconductor - Bill Spreen
 - ◆ Non-committal but maybe
 - ◆ Conference call April 12th

VITA 2.1-199x Task Group - Preliminary Working Document

- Can be found at URL: <http://www-ese.fnal.gov/vipa/ETL21rqns.pdf>