

Managing BGn* and IACK* During Live Insertion

Section 4.2 of draft 0.6 of the VITA 1.4 Live Insertion for VME64x standard describes a backplane circuit that manages the BGn* and IACK* daisy-chain signals. The circuit is normally turned on, connects the BG[0:3]in to the BG[0:3]out signals, and connects the IACKin* to the IACKout* signal for a given backplane slot. When the VMEbus board is capable of managing its daisy-chain signals the VMEbus board waits for the BG[0:3]in and IACKin signals to go inactive and then drives the LI/O signal low to disable the backplane daisy-chain circuit. At this point the VMEbus board is managing the daisy-chain signals.

Because the LI/O signal is on the D row of the 160 pin backplane connector the backplane daisy-chain circuit will only work with VME boards that have 160 pin connectors.

I was recently asked if the Force Computers GmbH electronic daisy-chain circuit would work with VITA 1.4 Live Insertion. The Force Computers circuit senses when the VMEbus board is driving a BG[0:3]out* or IACKout* daisy-chain signal, does not need the LI/O signal, and therefore will work with VMEbus boards that have 96 or 160 pin connectors. This patented (US #5,293,589) circuit was licensed to VITA members for \$1 so it meets the VSO patent policy.

The Force Computers electronic daisy-chain circuit is shown in Figure 1 below. The OR-gate #24 (this is an ISO formatted schematic) is usually a HCT part.

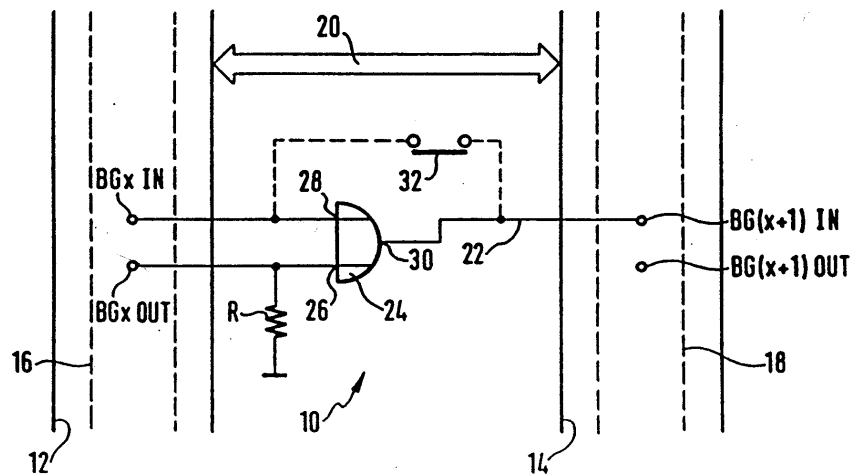


Figure 1, Force Computers GmbH Electronic Daisy-Chain Circuit

When the VMEbus board is first installed in an active VMEbus system the transceivers are in a high-impedance state and do not drive the BGx OUT signal. The resistor R keeps the BGx OUT signal low and therefore the BG(x+1) IN signal tracks the BGx IN signal. After the VMEbus board is initialized and the transceivers are enabled the BGx IN and

BGx OUT signals will be interconnected by the transceiver on the VMEbus board. When the VMEbus board requests control of the VMEbus it drives the BGx OUT signal high causing the bus grant signal to stop at this slot.

It looks like this circuit will work with VITA 1.4 Live Insertion, but I am concerned about a possible glitch on the BGx OUT line. If the BGx IN signal was low and the BGx OUT signal glitched high during insertion of the VMEbus board the BG(x+1) IN signal would glitch high. The downstream VMEbus board would see it's BGx IN signal low, glitch high, and then go low again.

Would the glitch on the BGx IN cause a problem?

What value of pull-down resistor R would be required to insure that the BGx OUT signal does not glitch high?

Are there any other problems with using this circuit with VITA 1.4 Live Insertion?

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