

TO: VSO-Member Connector Manufacturers
FROM: VITA 46 Working Group
DATE: 23-June-2003
SUBJECT: Request For Information Regarding a Legacy Supporting Connector Set

The purpose of this Request For Information (RFI) is to solicit information on a new VME P1/P2 pin-type connector that will increase the general purpose I/O pin count from that provided by the 5-row connectors, and a P0 receptacle connector that will support frequencies compatible with the next generation of serial fabrics (10 GHz). VITA 46 backplanes must be capable of accepting pre-VITA 46 VME boards without modification, but pre-VITA 46 backplanes do not have to support VITA 46 VME boards. In order to get the ball rolling we have submitted design concepts for a 7-row VME P1/P2 connector and a new P0.

P1/P2

Conceptually the base design for the 7-row P1/P2 connector starts with the current VME64 5-row connector and adds pins in the interstices between rows A&B and B&C. The interstitial pin rows are named, AB and BC. AB and BC pins may be the same size as used on the Metral-style 2mm connectors used for cPCI. One of the problems associated with these size pins is bending due to board to backplane misalignment. The proposed 7-row VME overcomes this problem by moving the mating plane of AB and BC behind that of rows A, B, and C. This results in four stages of alignment as illustrated:

1. Card guides provide coarse board alignment for connector engagement (not shown).
2. Connector engagement entry ways provide finer alignment for the large pins (A, B, C, D, Z)
3. A, B, C guide ways and A, B, C pin tapers align A, B, C, D, and Z rows and inherently align the connector so that rows AB and BC are within their guide way and pin taper tolerance range.
4. AB and BC guide ways and AB, BC pin tapers guide AB and BC pins into their respective positions.

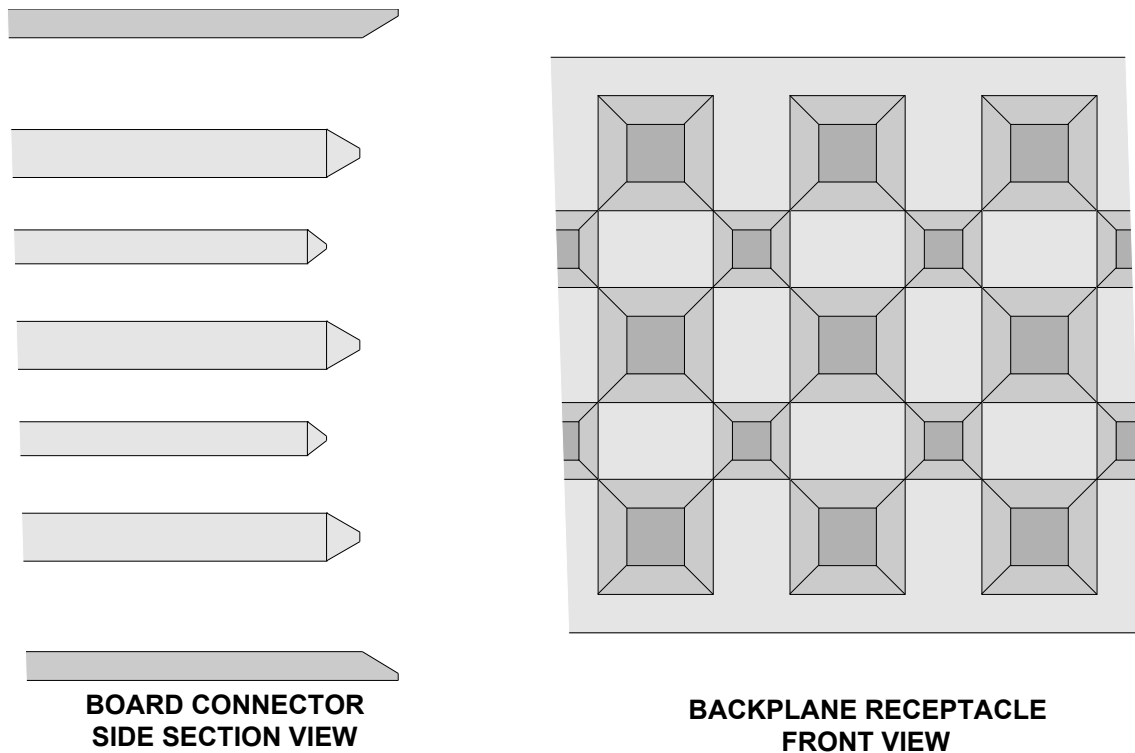


Figure 1. P1/P2 Concept Drawing

A VITA46 backplane uses the receptacle of Figure 1. The new backplane therefore supports both new and legacy VME boards. The interstitial pins provide an additional 62 general purpose I/O connections (124 total for both P1 and P2). One possible issue is crosstalk between these new pins and the VMEbus signals. This is not perceived to be a problem since the general purpose I/O pins are generally categorized as low frequency, but we will need a rough order of magnitude crosstalk estimate at 10 MHz.

P0

The VME board uses a receptacle connector in the P0 position and a pin connector in the backplane Jn0 position. In order to guarantee legacy support the Jn0 connector can not add any pins that would protrude into a legacy board's P0 receptacle. However, the new P0 connector will need a higher frequency capability for differentially paired signals than that which is supported by the current P0.

Figure 2 shows a possible way to obtain this capability using metallic or metalized plastic wafer shells around each receptacle. Each column uses identical interlocking wafers with the final column on the left being covered by an end cap. Not shown is the outer two rows which don't exist on P0 but do exist on Jn0. One of these rows, P0-H, should be consistent with the shell that is currently utilized on the existing P0 connector. The intent of the H-row contacts of Jn0 is to connect the shells to logic ground to complete the coaxial connections. The P0 connector also provides an H-row shell, not shown in Figure 2 that contacts the H-row pins of Jn0.

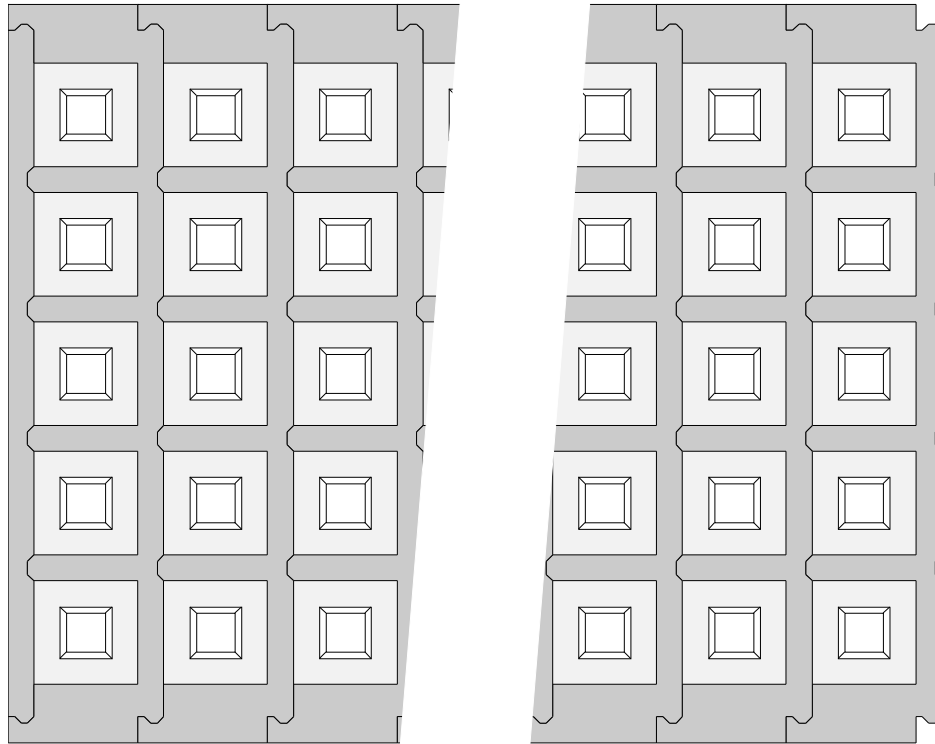


Figure 2. P0 Connector Face, Columns 1 to N

Each wafer requires internal insulators to keep the receptacles from contacting the metal shell (or metalized plastic shell). Figure 3 provides a representative design with a portion of the end cap and wafer body cut away to show the insulator and rib details. For clarity the figure shows the front view at the right of the wafer with the end cap installed. This design may be able to push the frequency capability of the P0/Jn0 connector combination (new P0, old Jn0) to 10 GHz without compensation while minimizing crosstalk between pins.

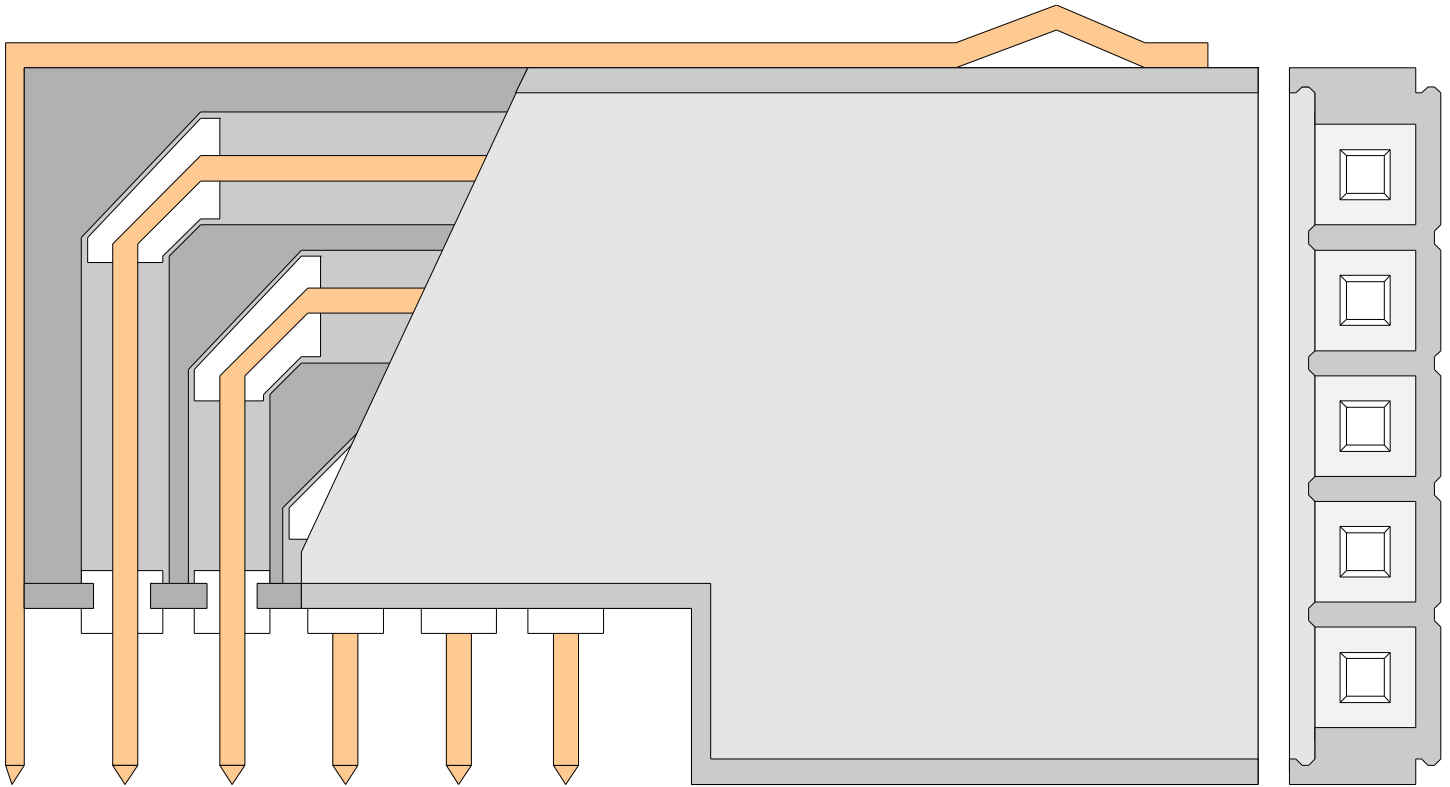


Figure 3. VITA 46 P0 Wafer Concept

Intellectual Property (IP)

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Information Desired From Connector Manufacturers

P1/P2 (7-row connector)

1. Rough order of magnitude (ROM) of pin to pin cross-talk with a 10 MHz, 10mA(rms) signal.
2. ROM for the development time
3. Earliest possible development start date

P0 (coaxial-style connector)

1. ROM of the frequency capability of the proposed or an alternative P0 connector
2. ROM for the development time
3. Earliest possible development start date