



# Vita 42.4 Working Group Proposal

HyperTransport  
Protocol Layer Standard



# Introduction

- HyperTransport™ (HT) is a very high speed, point-to point, low latency, packet-based interface designed primarily for component interconnect. Typically, it is used between a high-performance integrated microprocessor and other components, or between multiple microprocessors.



# HT Background

- AMD provided the initial specification for HyperTransport Technology, originally called “Lightning Data Transport”.
- Freely available specification maintained and enhanced by the HyperTransport Consortium, an open, member supported organization.



# HyperTransport Characteristics

- Efficient, low overhead, robust packet structure.
- Scalable Performance
  - Independent TX and RX Channels (Links)
    - Unidirectional
    - 2x, 4x, 8x, 16x and 32x Lanes Specified
  - 200, 300, 400, 500, 600, 800MHz, +++
    - DDR Data Transfer
    - Differential “LVDS – Like” (1.2V)



# HyperTransport Signals

- Command/Address/Data
  - CAD(R/T) [31,15,7,3,1:0]+/-
- Unidirectional Clock
  - CLK(R/T)+/-
  - 1 CLK for each 8-data bits
- Control
  - CTL(R/T)+/-
  - Used to identify Command Packet
  - 1 CTL per Link Direction



# HT Component Types

## ■ Tunnels

- Connect HT-to-HT

- May be different Link Width, Clock Freq

## ■ Bridges

- Connect HT to other Buses

- Like PCI, PCI-X

## ■ Caves

- HT to “Function Modules

- Like HT to AGP, GbE, LPC, etc.



# HTX Precedent

- HTX (HyperTransport eXpansion) specification recently released.
- First “plug-in” version of HT
- Hopefully will drive additional semiconductor development w/HT functionality



# HT Product Sampling

- AMD – Opteron™ 64-bit Processors
  - Scalable 1,2,4 and 8-way
  - Multiple Cache-coherent HT Links
- PMC-Sierra MIPS64™ Integrated uPs
- Broadcom Network Processors
- Transmeta Efficeon™ x86 Processors
- Alliance Semi. HT Tunnels and Bridges
- PLX HT-Dual PCI-X Bridge
- ULi, nVIDIA and AMD SouthBridges



# VITA 42 and HyperTransport

- XMC could support 2x, 4x, 8x and 16x Link topologies
- Both Peripheral and Processor XMC types possible
- Leverage efforts of Vita 42.x
  - Similar requirements to 42.3, PCI-E
  - Similar pin assignments



## Justification for V42 WG Effort

- HyperTransport is an OPEN standard for high performance semiconductor interconnect.
- HyperTransport will certainly have a place in embedded bus and board markets
- We'll have a lot of fun!



# What's Next

- Sponsors as of 1/20/2005

- Critia Computer, Inc.

- Advanced Micro Devices



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Thank you VITA and VSO Participants