

VMEbus FAQs- Frequently Asked Questions for the Beginning VMEbus User

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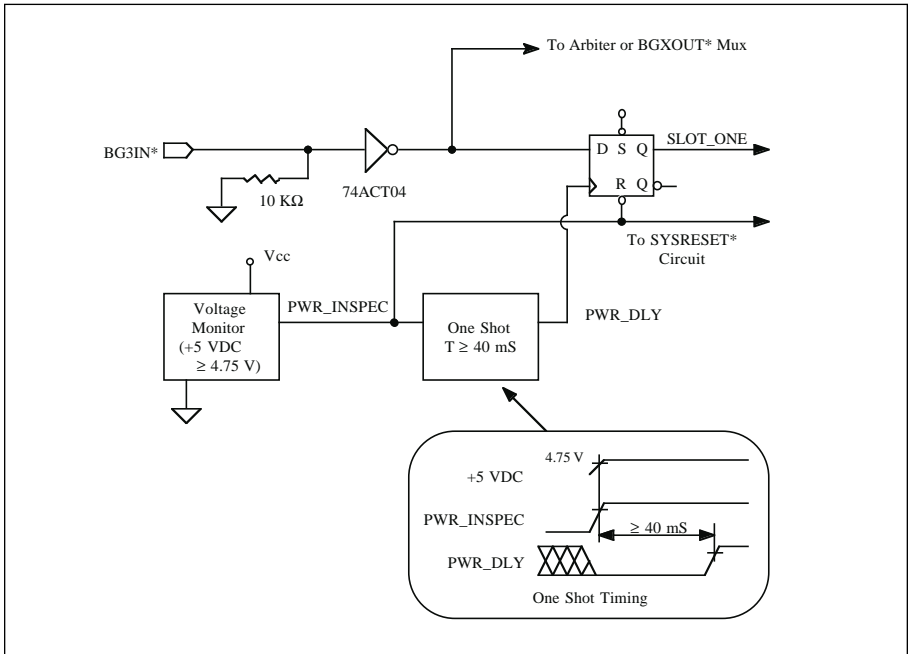
Question: What is the Auto SysCon Enable feature in the ANSI/VITA 1-1994, VME64 Standard?

The system controller function in the VMEbus provides for bus arbitration, a 16 MHz system clock, and the IACK daisy chain driver. A VME system should have one and only one system controller and according to the standard this function must reside in slot one of the backplane.

Originally, many systems contained a single module in slot one with system controller functions. However, because slot space is valuable and because the logic to implement a system controller is straight forward, most contemporary CPU boards provide a system controller that can be enabled or disabled depending where the module is placed. If it is placed in slot one then the system controller is enabled. If it is placed in any other slot besides slot one then the system controller function is disabled.

In the beginning, the VME standard assumed that the system controller function would be enabled or disabled via a hard wired jumper. However, many years of field experience have shown that it's not unusual for the system controller function to be misjumped so that a system ends up with either no system controller or multiple system controllers enabled and that the system either doesn't operate at all or it operates erratically.

The first slot detector was added to the ANSI/VITA 1-1994, VME64 standard, to provide a method for automatically enabling one and only one system controller. The first slot detector is the name given to the logic that is to reside on a module with auto system controller enable capability. Section 5.8 of ANSI/VITA 1-1994 VME64 Standard provides the requirements for the Auto System Controller enable feature. There are four rules and one observation. They are:



First Slot Detector Circuit

RULE 5.19:
Autoconfigured System Controller MUST NOT drive BG[3..0]IN*, or SYSCLK until the First Slot Detector (FSD) asserts SCON indicating that this board is the System Controller.

RULE 5.20:
An Autoconfigured System Controller MUST follow the power-up sequence requirements shown in Table 5 - 1.

RULE 5.21:
An Autoconfigured System Controller's Backplane Interface Logic MUST have a pull down on BG3IN*. (See Suggestion 6.9).

OBSERVATION 5.14:
It is necessary to use BG3IN* for the First Slot Detector because BG3IN* is the only bus grant input signal associated with a minimum function Arbitrator.

RULE 5.22:
Once an Autoconfigured System Controller becomes the System

Controller, it MUST remain the System Controller until after SYSRESET* is detected low or the system is powered down. If an Autoconfigured System Controller does not become the System Controller after powerup, it MUST remain in the non-System Controller state until after SYSRESET* is detected low or the system is powered down.

Also, in section 5.8, the standard states: "The FSD (first slot detector) delays POWER INSPEC for forty milliseconds to allow for board-to-board Power Monitor variations, then latches the state of BG3IN*. If BG3IN* is low, the FSD asserts SCON to enable the System Controller functions. If BG3IN* is high, the FSD keeps SCON deasserted to maintain the on-board System Controller in the inhibited state."

The first slot detector logic on a module uses the fact that BG3IN* in slot one is not connected to anything on the backplane. BG3IN* in all other slots will be dri-

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New Products Gallery

AP Labs was recently awarded a \$700,000 contract by Raytheon Service Co., Manchester, N.H., for the design and delivery of shipboard Vertical-Launch Interface Processor (VIP) systems. The shipboard VIP systems will be used by Raytheon for the Mark 48 Anti Ship Missile Defense System for an international customer.



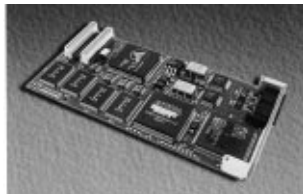
The VIP system utilizes a rack-mounted VME-based fully MIL qualified shipboard enclosure integrated with Commercial-Off-The-Shelf (COTS) hardware and software products. AP Labs may be found at: www.sd.aplabs.com

C-MAC Interconnect (Harlow, Essex, UK and West Palm Beach, Florida), a global manufacturer of custom-made, fully integrated backplane assemblies, announces the immediate availability of its advanced technology VSB and VXIbus backplanes.

VSB Backplanes allow a VMEbus processor board to access additional memory and I/O over a local bus, an essential feature in today's increasingly sophisticated and demanding system designs.

The company makes available a 300-page VME/VXI design guide which can be obtained by contacting Mort Thayer, C-MAC of America (Backplanes Division) Inc, 1601 Hill Avenue (West Wing), West Palm Beach, Florida. Tel: (407) 845 8455

A new PMC-based host bus adapter has been introduced by **DY 4 Systems**. The PMC-640 mezzanine card maximizes the superior communication and interconnection capabilities of ANSI Standard Fibre Channel for mission-critical applications that require high data throughput, low-latency, real-time transfers and minimized host processor overhead.



Fibre Channel makes it possible for the PMC-640 to deliver the high-speed and interconnect versatility required by data-intensive applications, such as digital signal processing, radar/sonar, network backbones, system clustering, video and image processing and map display systems. While the mezzanine card can be used with any SBC supporting PMC, it is especially designed for compatibility with DY 4's SVME-178 PowerPC based SBC and SVME-190 Pentium™-based SBC.

DY-4 is on the web at: www.dy4.com.

Joeger Enterprises Inc. has announced the Model VTR3012A, a 4 channel, 30MHz, 12 Bit Transient Recorder, packaged in a single width VME module. It features 4 independent channels, each with recording speeds to 30MHz with 12 bit resolution. It features SRAM storage of 2M words of data per channel, 8M words total. To improve readout speeds 2 channels are read at a time. The module can be programmed to operate in pre/post trigger, burst mode or multi-burst mode. To insure good system performance the active memory size, the gate duration size and single or "wrap" memory modes are selectable. To make maximum use of the high speed digitizing speed the input bandwidth is over 30MHz insuring accurate recording of analog waveshapes including pulse type signals. When band-

width limiting is required signal filters are employed. To ensure good noise immunity and high channel isolation each channel is filtered and uses its own ground plane. A programmable crystal oscillator is provided or an external clock can be used. The module has an interrupt structure and block transfer mode. Full scale input offset is provided allowing a wide range of signals to be handled. System software is available to simplify installation and use.

Joeger Enterprises, 166 Laurel Road East Northport, New York 11731. Tel: 516-757-6200, email joeger@bocom.com

The Model VT960, VME 96 input Time-to-Digital Converter, is the first of a series of new products from **LeCroy** using the VME64 standard (ANSI/VITA 1-1994). It incorporates features which are to be part of both the VME64 extensions (work currently in progress under VITA) as well as the VMEbus for physics specification currently being approved by the VME International Physics Association (VIPA). Applying this VME64 standard and a 9U style card makes the VT960 an economical but very powerful, universal TDC to be operated in an entirely VME environment. The key to the VT960's performance is the LeCroy MTD133B; a custom monolithic 500 psec, 8 input TDC integrated circuit. Sixteen hits (rising and/or falling edges) per channel, built-in zero suppress-



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ven high by the BG3OUT* from the preceding module. Thus by putting a pull down resistor (RULE 5.21) on the modules BG3IN* signal, BG3IN* will be sensed low in slot one and high in all other slots.

The FSD circuit shown on page 17 is taken from the 4th Edition of the VMEbus

Handbook by Wade Peterson. See Figure 5-14 on page 190 of the handbook. Wade has built and tested this circuit and states that "The first slot detector requires that BG3IN* be monitored with a low input current IC. If a standard totem-pole IC (such as a 74LS04) is used, the pull-down resistor may not work very good. " In the

example Wade suggests a 74ACT04 as a better choice.

The auto syscon enable feature was added to the ANSI/VITA 1-1994, VME64 Standard to make system configuration easier and more reliable. The addition of this feature is an example of the continuing evolution of the VMEbus to meet ever changing needs.