

# VMEbus FAQ's-

## Frequently Asked Questions for the Beginning VMEbus User

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**Question? The VMEbus provides a variety of addresses spaces and data widths. Why are there so many modes and how do they relate to each other?**

### Address Spaces

The VME64 specification, ANSI/VITA 1-1994, VME64, which received ANSI recognition on April 10, 1995, provides for 16 bit, 24 bit, 32 bit, 40 bit and 64 bit address spaces. These address spaces are known respectively as A16, A24, A32, A40, and A64. A six bit address modifier code is used to distinguish between these address spaces. When the master in a VMEbus system wants to generate an address in the A16 address space, for example, it must put out the proper address modifier code. This code tells all boards on the bus that this address cycle is in A16 address space.

A16, also known as short I/O address space, provides for 64Kbyte of addressing and was put into the specification to reduce address decoding for simple I/O boards. Since most simple I/O boards contain only a handful of registers a 64Kbyte space was deemed sufficient.

The A24 address space only requires the P1/J1 VMEbus connector. Hence it is the standard address space used by 3U VMEbus modules which only have a P1 connector. 24 bits provides a 16 Mbyte addressing space which was a lot in the early 1980's when VMEbus was first released. A24 is quickly becoming a legacy issue since it is not used on 6U boards today.

The P2 connector is used to provide the additional address and data lines needed to access 32 bits in non multiplexed mode. While many early 6U VMEbus modules with only a P1 connector used A24 address space, most contemporary 6U cards with both P1 and P2 connectors use A32 bit as their main

address space. A32 provides 4 x 10<sup>9</sup> bytes of addressing space.

A40 is defined in the VME64 specification to allow for additional addressing space on 3U modules by multiplexing the 24 bit address bus with the 16 bit data bus.

A64 is defined in the VME64 specification to allow for additional addressing space on 6U modules by multiplexing the 32 bit data bus with the 32 address data bus to produce a 64 bit address cycle. A64 provides for 1.845 x 10<sup>19</sup> bytes of addressing space. (Hopefully such a large space will be sufficient for the next several years, but then one never knows.)

VMEbus processor modules will map each of these address spaces into their processor's memory space. While not part of the VME64 specification, usually on-board local memory is positioned at address location 0 with on-board I/O positioned in high memory starting at locations above 0xF000 0000. The address space in between usually maps to one of the VMEbus address spaces. On some boards these address space assignments may be hardwired into the logic or set manually with jumpers while on other boards these address space assignments may be programmable.

### Data Transfer Cycles

The VME64 spec provides for 8 bit, 16 bit, 32 bit, and 64 bit data transfer cycles. Besides width, data transfer cycles can be either single cycle or block transfer. Single cycle means that an address is sent with each data transfer while block transfer means that one address is sent with multiple data transfers. The original implementation of the VMEbus used non-multiplexed buses to achieve 32 bit addresses and 32 bit data transfers utilizing both P1 and P2 connectors. In 1989 it was realized that both the address bus and the data bus could be doubled from 32 bits to 64 bits by multiplexing without requiring additional pins. The VME64

specification brings multiplexed address and data cycles to both P1 only and P1/P2 configurations.

Single cycle data transfer operations are labeled D8(O), D8(E0), D16, D32, and MD32. A D8 cycle can be either D8 (O) odd address or D8 (EO) even and odd address. From a hardware standpoint a 16 bit word is the basic unit on the VMEbus. Two data strobes, DS0\* and DS1\* are used to select either the low byte, the high byte, or both bytes within a 16 bit word. D8(O) provides for addressing odd address bytes only. This reduces address decoding requirements for simple I/O boards but provides for accessing only the odd bytes in a defined memory space. On the other hand D8(E0) provides for access to both odd and even bytes. D16 accesses require only the P1 connector while D32 accesses require both the P1 and the P2 connectors. MD32 stands for multiplexed 32 bit transfers and is used primarily on 3U modules to transfer 32 bits by multiplexing 16 bits of data on 16 of the possible 23 address lines. MD32 allows a 2x speed enhancement using only the P1 connector.

Block transfer operations improve data transfer efficiency by sending only one address for multiple bytes of data. These block transfer operations are labeled BLT, MBLT, and A40 BLT. BLT (Block Transfer) operations provide for data width transfers of 8 bits and 16 bits on P1 and 8, 16, and 32 bits on P1/P2. BLT is part of the original VMEbus specification. MBLT (Multiplexed Block Transfer) was added to the VME64 specification to allow 64 bit transfers by multiplexing data onto the 31 address lines (A1-A31) and the LWORD\* control line. MBLT requires both the P1 and the P2 connector. A40BLT (A40 Block Transfer) provides for 8, 16, and 32 bit multiplexed block transfers on a P1 only module and was added primarily for 3U module use.

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ment nor any software to buy and constantly upgrade. RTnet products are based on the very simple concept of using a high-speed, fiber-optic network board as a memory device, a PLC accelerator, or as an extremely high-performance database sharing network. Products from VMIC's RTnet family have been proven in aircraft and nuclear power plant simulation, and in industrial applications including aluminum rolling mills, test and measurement applications and high-speed radar and missile systems.

VMIC's RTnet products allow data to be shared among as many as 256 independent systems (nodes). Reflective Memory technology, when used as a database sharing network, allows PLCs, CPUs, and other controllers to gather, collate, and distribute information to any node on the ring without the compatibility problems incurred when using dissimilar systems.

RTnet products create a real-time, memory-based network which transfers all data to a node's local memory where it is simultaneously stored in that board's dual-port memory and sequenced out to all the other nodes' memory. There are no software delays and minimal hardware delays associated with the data transfer. The VMIC 5588 family of fiber-optic RTnet products take only 700 ns per node for the data to be stored in and transmitted out of each node; whereas, the VMIC 5576 family of RTnet products have a latency of 1,200 ns. Using RTnet products in distributed multiprocessing systems brings the level of performance to heights not possible with traditional off-the-shelf communication technologies.

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**Software Systems Engineer-** Situated in Silicon Valley, you will be responsible for ensuring that the individual needs of our customers are met through the application of software tools, company knowledge and individual software development expertise.

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Support of pre sales presentations as required.

Experience with real time embedded computing either digital signal processing or single board computing. Strong track record of software development accomplishments. VME experience is highly desirable as is knowledge of real time operating systems such as Lynx and / or VxWorks.  
Knowledge of PowerPC is a plus for this position.

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### Mixing Different Address and Data Widths

The VMEbus specification allows different address and data widths to be used based on an application requirement. While all combinations are possible, certain combinations are more common than others. For example, A16/D8(O) is common for simple I/O boards while A32/D32 and A32/D64 are common for high performance SBC modules. As stated earlier A24 is usually found only on older 6U modules and is quickly being replaced by A32.

Regarding interoperability between modules with differing address and data capabilities, the VME64 specification states the following:

RULE 2.76 D16 Slaves MUST include D08(E0) capability.

RECOMMENDATION 2.3 D16 Masters should include D08(E0) capability.

RULE 2.77 D32 and MD32 Slaves MUST include D16 and D08(E0) capabilities.

#### RECOMMENDATION 2.4

D32 and MD32 Masters should include D16 and D08(E0) capabilities.

#### RECOMMENDATION 2.5

MBLT Masters should include D32, D16 and D08(E0) capabilities.

Manufacturers must follow RULES to be in compliance and should follow RECOMMENDATIONS to offer optimum interoperability.

### Summary

The VME64 specification provides a variety of data transfer capabilities from single cycle 8 bit transfers to multi-cycle 64 bit transfers. In addition, address spaces from 16 bits to 64 bits provide complete flexibility while reducing design complexity. With these capabilities the VMEbus can meet a wide range of system requirements.

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